PCI/104-Express™
&
PCIe/104™
Specification

Including Adoption on
104™, EPIC™ and EBX™ Form Factors

Version 2.10

February 18, 2013

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REVISION HISTORY

March 21, 2008 Version 1.0

- Initial release

March 27, 2009 Version 1.1

- Add USB and over current signal to pin out, inserted description in 1.4.4, modified shift example to include USB
- Section 2.4 corrected that even numbered pins are located towards the inside of the board and odd numbered pins are located towards the edge of the board
- PEx16_ENA changed to PEG_ENA# in section 2.4.1.2 and 2.4.3
- Figure 2.3 Moved Host to bottom in this figure and added USB
- Figure 6-14 Top two boards are PCI/104-Express

February 10, 2011 Version 2.0

- Added Type 2 connector version
- Added 22mm connector option
- Removed Figure 6 4: Mating of Top Half and Bottom Half of Connector A because this non-dimensioned sketch provided no useful information
- Editorial changes:
    - Changed signal names PWRGD to PWRGOOD, CPU_DIR to DIR, and 5V_Always to +5V_SB for consistency
    - Corrected USB0 and USB1 in Automatic Link Shifting Examples for Host and Various Devices
    - Corrected text in Appendix B and C related to PCI/104-Express Expansion Zone
    - Redrew Example breakout routing of connector bank 1 PCI Express x1 links with shifting
    - Changed PCIe to PCI Express when discussing the PCI Express specification.
    - Cleaned up drawings in Figure 1-1
    - Swapped order of section 1.3 and 1.4 and edited text
    - Fixed missing references.
    - Added signal switches suggestions for SATA and USB 3.0

March 21, 2011 Version 2.01

- Provided SATA definitions that were omitted in previous version.

February 18, 2013 Version 2.10

- Corrected Consortium name in all references
- Expanded introduction to PCI Express to include Gen 1, 2, and 3.
- Added PCI Express Gen 2 recommendations.
    - Added devices and updated signal switch table.
    - Updated layout recommendations section to include PCIe Gen 2 & 3.
    - Added Gen 2 & 3 to via and trace length table.
    - Removed microstrip and stripline examples.
- Added PCI Express x4, x8, and x16 layout examples.
- Added SATA and USB 3.0 capacitor info and layout examples.
- Changed SDVO to Alternate Function

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Glossary of Terms

Terms	Definitions
ATX	Advanced Technology Extended A specification for PC motherboards, power supplies, and system chassis. One of its most notable features is support for "Standby" and "Soft-Off" power savings modes.
Device	A logical device attached to a PCI Express Link. Generally an add-in card.
DMA	Direct Memory Access A method for peripherals to efficiently access system memory without CPU intervention.
EBX	Form factor for SBC's
Host	The central connection of a PCI Express system, typically a CPU module. This is called the "Root Complex" by the PCI Express specification.
ISA Bus	Industry Standard Architecture A legacy bus used on earlier PCs. It has been phased out of desktop PCs, but is still common in embedded systems.
Lane	Fundamental unit of a PCI Express connection. A set of differential signal pairs, one pair for transmission, and one pair for reception. Multiple lanes may be combined to increase bandwidth (up to x16). A "by-N Link" is comprised of N Lanes.
Link	The collection of one or more PCI Express Lanes, plus an additional differential pair for a clock, which make up a standard PCI Express interconnect. According to PCI Express Specification 1.1 a Link can be comprised of 1, 4, 8, or 16 Lanes.
Packet Switch	A device used to attach multiple PCI Express devices to a single link on the HOST. The PCI Express Specification refers to this simply as a "Switch." In this document, the term "Packet Switch" is used to differentiate from a "Signal Switch."
PCIe	PCI Express
PEG	PCI Express Graphics
SBC	Single Board Computer
SDVO	Serial Digital Video Output used from Intel 915/945/965 chipsets
Signal Switch	An analog switch used to select between multiple PCI Express devices to attach to a single PCI Express link, or multiple links to attach to a single device. Also called a "Channel Switch."
SMBus	System Management Bus
USB	Universal Serial Bus
LPC	Low pin count bus, a bus specification for legacy devices
SATA	Serial ATA Bus

1. INTRODUCTION

1.1. Purpose

This document defines the addition of PCI Express, the next generation serial interconnect bus, to the stackable 104, EPIC, and EBX form factors. PCI Express was chosen because of its performance, scalability, wide market acceptance, and growing silicon availability worldwide. The PCI Express architecture uses familiar software and configuration interfaces of the conventional PCI bus architecture, but provides a new high-performance physical interface while retaining software compatibility with the existing conventional PCI infrastructure.

PCI Express is a high performance I/O architecture used in both desktop and mobile applications. This hierarchical, point-to-point interconnect works well with on-board and slot oriented architectures. The purpose of this Specification is to adapt PCI Express to the stacked architecture employed with 104, EPIC and EBX form factors.

1.2. Standard Identification

A PCI-104 board with the addition of PCI Express becomes PCI/104-Express. A board with only the PCI Express connector is called PCIe/104. Each of these configurations can be applied to EPIC and EBX as shown in Appendix B and C. This allows full interchangeability with add-in devices across all PC/104 form factors.

1.3. Description

As computer technology continues to develop, the PC/104 community must expand to the new, widely accepted and sustained technologies of the day. The PCI/104-Express Specification provides this next generation PC/104 platform with a connector architecture that provides high-speed interfaces, maintains the ability to develop low-cost modules, and is sustainable for the foreseeable future.

Key to its development was obtaining a high speed, 3-bank, stackable PCI Express connector for both up and down stacking, while retaining the stackable PCI connector for backward compatibility to PCI-104, PC/104-*Plus*, and PC/104 peripheral modules. Figure 1-1 shows a basic view of the PCI/104-Express and PCIe/104 layouts.

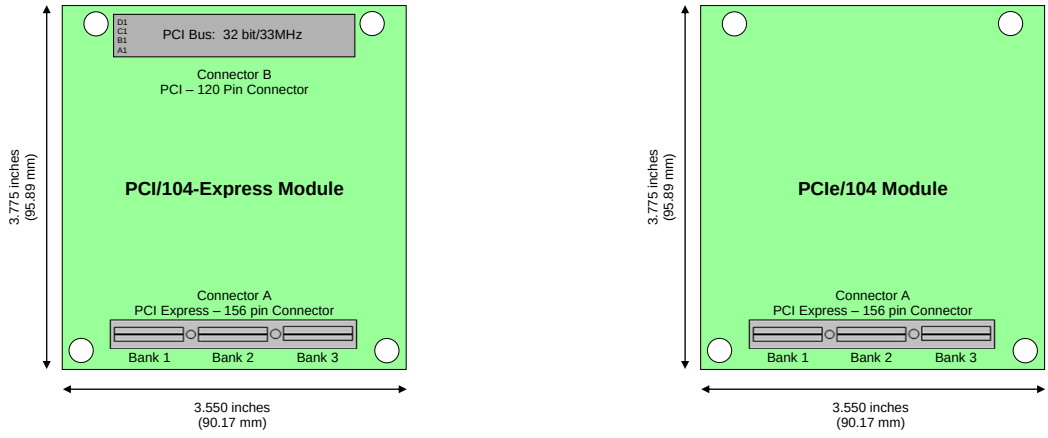

Figure 1-1: PCI/104-Express and PCIe/104 Board Layouts on 104 Form Factor

ISA bus backward compatibility can naturally and easily be achieved with the use of a PCI-to-ISA bridge peripheral module (see Appendix A).

1.4. PCIe/104 Type 1 and Type 2

PCIe/104 is implemented by a pair of high-speed surface mount connectors which is a major change from the through board stacking connectors used by PC/104 and PCI-104. If the host CPU has top and bottom connectors electrically connected together then the system can be built either stack-up or stack-down, but not both at the same

time. However, there is no requirement for the connector on the top of the host to be electrically connected to the connector on the bottom of the host. This means that a PCIe/104 bus stacking up can be completely separate from PCIe/104 bus going down. The specification does require all peripheral boards to be universal, so all peripheral boards will work either above or below the CPU.

This specification defines two versions of the PCIe/104 connector pin out, Type 1 and Type 2. Type 1 is the same versions 1.0 and 1.1 of the PCI/104-Express and PCIe/104 specification. Type 2 replaces the PCI Express x16 link with two PCI Express x4 links, two USB 3.0, two SATA, LPC, and an RTC battery. See Table 1-1 below for a comparison.

Table 1-1 Feature Summary

Feature	Type 1	Type 2
USB 2.0	2	2
SMB	1	1
PCIe x1	4	4
PCIe x4		2
PCIe x16*	1	
USB 3.0		2
SATA		2
LPC		1
RTC Battery		1

* x16 Link can be used as x8 or x4, see section 2.4.1.1

1.4.1 PCI/104-Express Version 1.0 and 1.1 Host Board Compatibility

All host boards built to version1.0 and 1.1 boards are considered Type 1.

1.4.2 PCI/104-Express Version 1.0 and 1.1 Peripheral Board Compatibility

All PCI Express x1, USB 2.0, and SMBus boards build to version 1.0 or 1.1 are considered Universal boards and will work unchanged on either Type 1 or Type 2 host CPUs. PCI Express x16 peripherals work only on Type 1 hosts. USB 3.0, SATA, and LPC peripherals will work only on Type 2 hosts.

The PCIe/104 connector is composed of three banks of pins. Bank 1 has pins 1– 52, Bank 2 has pins 53 – 104, and Bank 3 has pins 105 – 156. The pin assignments on Bank 1 of the connector is exactly the same in Type 1 and Type 2, therefore all the PCI Express x1, USB 2.0, SMBus, and all the control signals are the same. Likewise all power and grounds are the same throughout the connector.

1.5. PCIe/104 Feature Set

1.5.1 Connector A : PCI Express Bus

Both PCIe/104 Type 1 and Type 2 have this common feature set and pin assignments:

- Four x1 PCI Express Links
- Two USB 2.0
- ATX power and control signals: +5V Standby, Power supply on, Power OK
- Power: +3.3V, +5V, +12V
- SMBus

Type 1 has the common feature set plus:

- One x16 PCI Express Link, or optionally two x8 Links, or two x4 PCI Express Links

Type 2 has the common feature set plus:

- Two x4 PCI Express Links
- Two USB 3.0
- Two SATA
- LPC Bus
- RTC Battery

1.6. PCI/104-Express Feature Set

1.6.1 Connector A : Same as 1.5.1 above

1.6.2 Connector B: PCI Bus:

- PCI Bus: 32 bit, 33 MHz, Four Bus Master capable (same as on PC/104-*Plus* and & PCI-104)
- +5V Standby, Power supply on, and power management event signals for ATX power supply
- Power: +3.3V, +5V, +12V, -12V
- Same location and pin out as PCI-104 and PC/104-*Plus* specifications

1.7. General Stacking Rules

This specification defines Type 1 and Type 2 host and peripheral modules. There are four stacking rules.

- Peripheral modules connecting with PCI Express x1 or x4 links, USB 2.0 links, or SMB are universal and can plug into either a Type 1 or a Type 2 host.
- Peripheral modules connecting with PCI Express x16 or x8 links must plug into a Type 1 host.
- Peripheral modules connecting with SATA, USB 3.0, or LPC links must plug into a Type 2 host.
- Any peripheral module plugged in the wrong bus holds the system in reset and causes no damage.

Guidelines for stacking PCI Express Gen 1, 2, 3, USB 3.0, and SATA.

- Build a stack by putting higher clock rate peripherals closer to the host. Follow the priority below:
    1. Gen 3 PCI Express at 8.0 Gigabits/second closest to the host
    2. SATA 3 at 6.0 Gigabits/second next closest
    3. Gen 2 PCI Express and USB 3.0 at 5.0 Gigabits/second
    4. SATA 2 at 3.0 Gigabits/second
    5. Gen 1 PCI Express at 2.5 Gigabits/second
    6. SATA 1 at 1.5 Gigabits/second
    7. USB 2.0 at 480 Mbit/second
- Follow the guidelines for up and down stacking in Table 1-2 Type 1 & Type 2 Combinations below.

For example, if you have a host with a Type 1 stacking down and a Type 2 stacking up with one SATA 2, one USB 3.0, one PCI Express x1 Gen 2, two PCI Express x1 Gen 1, and one PCI Express x16 Gen 2 peripherals your stack could be configured as:

- SATA peripheral
- USB 3.0 peripheral
- Host (Type 1 going down and Type 2 going up)
- PCI Express x16 Gen 2 peripheral
- PCI Express x1 Gen 2 peripheral
- PCI Express x1 Gen 1 peripheral
- PCI Express x1 Gen 1 peripheral

For details on host and peripheral configuration see section 4, PCIe/104 Type 1 and Type 2 Stacking.

1.8. Stack Up, Stack Down, and Both

If the host CPU has the same type connector on top and bottom of the board and the signals are connected together, boards can be stacked either up or down using the direction signal DIR to indicate to the peripheral board where the host is located. In this case, care must be taken not to stack boards in both directions because signal stubs will be created which may adversely affect the bus signals.

Surface mounted connectors permit the top and bottom connectors to be separate busses. If the host CPU is built with separate busses on top and bottom there will not be stubs when stacking cards both up and down at the same time. This specification supports connected or separate bus options as long as board configuration rules are followed. Table 1-2 shows the maximum number of links for all the possible combinations.

Table 1-2 Type 1 & Type 2 Combinations

PCIe/104	Type 1		Type 2		Type 1 & 2 Combo	
Top and Bottom Connectors	Connected	Separate	Connected	Separate	Connected	Separate
Peripheral Board Stacking	Either up or down	Both up and down	Either up or down	Both up and down	Not Allowed	Both up and down
x1 PCIe Links	4	8	4	8		8
USB 2.0	2	4	2	4		4
SMB	1	1	1	1		1
x4 PCIe Links	2	4	2	4		4
x8 PCIe Links	2	4	None	None		2
x16 PCIe Links	1	2	None	None		1
SATA	None	None	2	4		2
USB 3.0	None	None	2	4		2
LPC	None	None	1	1		1

1.9. Bus and Signal Group Descriptions

1.9.1 PCI Express Expansion Bus

PCI Express is a high performance, general purpose I/O interconnect defined for a wide variety of future computing and communication platforms. Key PCI attributes, such as its usage model, load-store architecture, and software interfaces, are maintained, whereas its parallel bus implementation is replaced by a highly scalable, fully serial interface. PCI Express takes advantage of recent advances in point-to-point interconnects, Switch-based technology, and packet-protocol to deliver new levels of performance and features. Power Management, Quality of Service (QoS), Hot-Plug/Hot-Swap support, Data Integrity, and Error Handling are among some of the advanced features supported by PCI Express. PCI Express has three signaling rates.

- Generation 1, Gen 1, is 2.5 Gigabits/second/Lane/direction of raw bandwidth
- Generation 2, Gen 2, is 5.0 Gigabits/second/Lane/direction of raw bandwidth
- Generation 3, Gen 3, is 8.0 Gigabits/second/Lane/direction of raw bandwidth

PCI/104-Express and PCIe/104 incorporate four x1 PCI Express Links and options for either a single x16 Link, or two x8 Links, or two x4 PCI Express Links to allow connections to standard PCI Express device chips. The x16 Link option allows maximum flexibility, configurability, and expandability for current and future designs. Some examples of x16 Link application are next generation graphics chips, 1/10 gigabit Ethernet chips, or use with a PCI Express Switch which can then branch the high throughput out into any number of various size Links including multiple x16 Link graphics engines. The only limitation is the bandwidth requirement for each of the branched links.

1.9.1.1 PCI Express x16 or PEG Link

PCI Express x16, sometimes called PEG (PCI Express for Graphics), is an interface with 16 PCI Express differential lanes to connect a high performance video controller or other high bandwidth devices. In chipsets with internal graphics, the PEG bus is used as an alternative to connect an external video controller. The internal chip controller is

disabled in this case. The PEG-Bus configuration must be enabled from the Device by connecting the PEG-ENA# signal to ground.

1.9.1.2 Non-PCI Express functions of the CPU/Chipset x16 Link

Some processors/chipsets allow alternate functions on the x16 link pins. There is no standard which all manufacturers follow, so this specification will not define one. Using these alternate functions is allowed, but it is up to the host board manufacturer to define the alternate uses and what peripheral boards are compatible. Use of the PEG-ENA# shall remain open on these peripheral boards.

One example of this is Serial Digital Video Output (SDVO). This bus is provided as an alternative to the PEG-Bus on some CPU chipsets. SDVO-Links needs up to 7 differential signal pairs per interface.

1.9.2 SATA Links

Serial ATA (SATA or Serial Advanced Technology Attachment) is a computer bus interface for connecting host bus adapters to mass storage devices such as hard disk drives and optical drives. Serial ATA was designed to replace the older ATA (AT Attachment) standard (also known as EIDE). It is able to use the same low level commands, but serial ATA host-adapters and devices communicate via a high-speed serial cable over two pairs of conductors. Support for device detection and power enable for hot-pluggable applications.

1.9.3 LPC Bus

The Low Pin Count bus, or LPC bus, is used on IBM-compatible personal computers to connect low-bandwidth devices to the CPU, such as the boot ROM and the "legacy" I/O devices. The "legacy" I/O devices usually include serial and parallel ports, keyboard, mouse, and floppy disk controller.

The LPC bus was introduced by Intel in 1998 as a substitute for the Industry Standard Architecture (ISA) bus. It resembles ISA to software, although physically it is quite different, replacing the 16-bit-wide, 8.33 MHz ISA bus with a 4-bit-wide bus operating at 4 times the clock speed (33.3 MHz). LPC's main advantage is that it requires only seven signals.

1.9.4 Universal Serial Bus (USB)

The USB is specified to be an industry-standard extension to the PC architecture with a focus on PC peripherals that enable consumer and business applications. The following criteria were applied in defining the architecture for the USB:

- Ease-of-use for PC peripheral expansion.
- USB 2.0 is a low-cost solution that supports transfer rates up to 480Mb/s.
- USB 3.0 is a high-speed solution with speeds up to 4800Mb/s
- Full support for real-time data of voice, audio, and video.
- Protocol flexibility for mixed-mode isochronous data transfers and asynchronous messaging.
- Integration in commodity device technology.
- Comprehension of various PC configurations and form factors.
- Provision of a standard interface capable of quick diffusion into a product.
- Enabling new classes of devices that augment the PC's capability.
- Full backward compatibility of USB 2.0 for devices built to previous versions of the specification.

The over-current protection is made on each PCI/104-Express peripheral board, if needed. Any channel can pull the OC#-Signal low to indicate the CPU host that an over-current situation has occurred.

1.9.5 System Management Bus

The optional System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate with each other and with the rest of the system. It is based on the principles of operation of I2C. SMBus provides a control bus for system- and power-management related tasks. A system may use SMBus to pass messages to and from devices instead of tripping individual control lines. Removing the individual control lines

reduces pin count. Accepting messages ensures future expandability. With SMBus, a device can provide manufacturer information, tell the system what its model/part number is, save its state for a suspended event, report different types of errors, accept control parameters, and return its status. SMBus is described in System Management Bus (SMBus) Specification, Version 2.0. Refer to this specification for DC characteristics and all AC timings. If the system board or add-in card supports SMBus, it must adhere to additional requirements that may be found in Chapter 8 of the PCI Local Bus Specification, Revision. 3.0.

An address resolution protocol (ARP) is defined in the SMBus 2.0 Specification that is used to assign slave addresses to SMBus devices. Although optional in the SMBus 2.0 Specification, it is required that systems that connect the SMBus to PCI slots implement ARP for assignment of SMBus slave addresses to SMBus interface devices on PCI add-in cards. The system must execute ARP on a logical SMBus whenever any PCI bus segment associated with the logical SMBus exits the B3 state or a device in an individual slot associated with the logical SMBus exits the D3cold state. Prior to executing ARP, the system must insure that all ARP-capable SMBus interface devices are returned to their default address state.

The system board provides pull-ups to the +3.3Vaux rail per the above specification and the components attached to these signals need to have a 3.3V signaling tolerance (5V signaling must not be used). Also, the SMBus is used during all power states, so all components attached to the SMBus must remain powered during standby, or ensure that the bus is not pulled down when not powered.

The SMBus interface is based upon the System Management Bus Specification (SMBus 2.0 Specification). This two-wire serial interface has low power and low software overhead characteristics that make it well suited for low-bandwidth system management functions.

The capabilities enabled by the SMBus interface include, but are not limited to, the following:

- Support for client management technologies.
- Support for server management technologies.
- Support for thermal sensors and other instrumentation devices on add-in cards.
- Add-in card identification when the bus is in the B3 state or when the PCI device is in the D3hot or D3cold states as defined in the PCI Power Management Interface Specification.

1.9.6 ATX and Power Management

PCI/104-Express and PCIe/104 incorporate all of the necessary control and signal lines for ATX and power management functionalities. These signals include PWRGOOD, PSON#, +5V_SB, and PME#. The inclusion of these signals allows maximum power savings.

PWRGOOD is a “power good” signal. It should be asserted high by the power supply to indicate that the +12 VDC, +5 VDC, and +3.3 VDC outputs are above the under-voltage thresholds and that sufficient main energy is stored by the converter to guarantee continuous power operation within specifications. Conversely, PWRGOOD should be de-asserted to a low state when any of the +12 VDC, +5 VDC, or +3.3 VDC output voltages falls below its under-voltage threshold, or when main-power has been removed for a sufficiently long enough time that the power supply operation cannot be guaranteed beyond the power-down warning time.

PSON# is an active-low, TTL-compatible signal that allows a motherboard to remotely control the power supply in conjunction with features such as soft on/off, wake-on-LAN, or wake-on-modem. When PSON# is pulled to TTL low, the power supply should turn on the five main DC output rails: +12 VDC, +5 VDC, +3.3 VDC, -5 VDC, and -12 VDC. When PSON# is pulled to TTL high or open-circuited, the DC output rails should not deliver current and should be held at zero potential with respect to ground. PSON# has no effect on the +5V_SB output, which is always enabled whenever AC power is present. PSON# shall be pulled to +5V_SB with a 10K ohm resistor on the power supply.

+5V_SB is a standby supply output that is active whenever AC power is present. It provides a power source for circuits that must remain operational when the five main DC output rails are in a disabled state. Example uses include soft power control, wake-on-LAN, wake-on-modem, intrusion detection, or suspend state activities.

1.9.7 RTC Battery

Any board in a system can provide a 3.0 to 3.6 volt battery on pin 154 of the Type 2 connector. This battery shall be current limited with a 1KΩ resistor, reverse current protected with a schottky diode, and filtered with a 10uF capacitor. Any board in the system may use the battery. Battery life will depend on the specific battery used and the load.

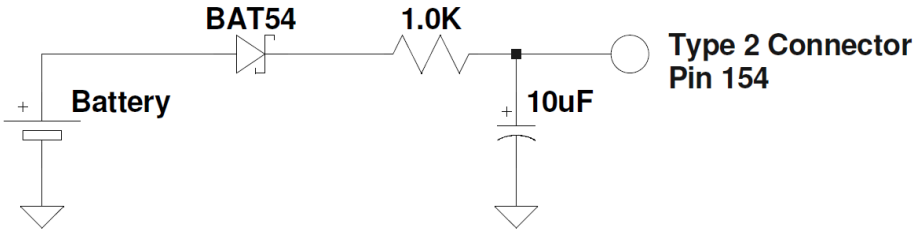

Figure 1-2 RTC Battery Example

1.9.8 PCI Expansion Bus

The PCI Expansion Bus is the same 32 bit, 33 MHz PCI bus found on the PC/104-*Plus* and PCI-104 Specifications with the addition of +5V_SB, PSON#, and PME#.

1.10. References

The following documents should be used as reference for a detailed understanding of the overall system requirements. For latest revisions of the above specifications contact the respective organizations.

PC/104 Specification	**PC/104 Consortium**	www.pc104.org
PC/104-*Plus* Specification	**PC/104 Consortium**	www.pc104.org
PCI-104 Specification	**PC/104 Consortium**	www.pc104.org
PCI Local Bus Specification Revision 2.2	**PCI Special Interest Group**	www.pcisig.com
PCI Express Base Specification Revision 1.1	**PCI Special Interest Group**	www.pcisig.com
ATX Specification Version 2.2	**Intel Corporation**	www.intel.com
System Management Bus (SMBus) Specification Version 2.0	**SBS Implementers Forum**	www.sbs-forum.org
INTEL description of PEG and SDVO in the 915/945/965 chipsets	**Intel**	www.intel.com
USB Specification Revision 2.0 USB Specification Revision 3.0	**USB Implementers Forum**	www.usb.org

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2. EXPANSION CONNECTOR A

2.1. Functions

Because not all chipsets support all PCI Express link configurations, it is up the Host manufacturer to determine the type and number of PCI Express Links to include in their expansion connector. However, the placement of these PCI Express Links must comply with the pin out described below for Connector A. This will ensure that any x1 or x4 or x8 or x16 PCI Express Device will work on any Host that has an x1, or x4 or x8, or x16, respectively.

2.1.1 PCIe/104 Type 1 and Type 2 Common Features

- Four x1 PCI Express Links
- Two USB 2.0
- ATX power and control signals: +5V Standby, Power supply on, Power OK
- Power: +3.3V, +5V, +12V
- SMBus

2.1.2 PCIe/104 Type 1 Only Additional Features

- One x16 PCI Express Link, or optionally two x8 Links, or two x4 PCI Express Links

2.1.3 PCIe/104 Type 2 Only Additional Features

- Two PCI Express x4 Links
- Two USB 3.0
- Two SATA
- LPC Bus
- RTC Battery

2.2. Signal Descriptions

2.2.1 PCIe/104 Type 1

Table 2-1 Connector A Type 1 Signals

Group	Pins	Signal Name	Host Direction	Description
PCIe x1	4	PEx1_[0:3]Tp	Output	Transmit Differential Upper Line for x1 Links 0, 1, 2, 3. Shifted when used.
	4	PEx1_[0:3]Tn	Output	Transmit Differential Lower Line for x1 Links 0, 1, 2, 3. Shifted when used.
	4	PEx1_[0:3]Rp	Input	Receive Differential Upper Line for x1 Links 0, 1, 2, 3. Shifted when used.
	4	PEx1_[0:3]Rn	Input	Receive Differential Lower Line for x1 Links 0, 1, 2, 3. Shifted when used.
	4	PEx1_[0:3]CLKp	Output	Clock Differential Upper Line for x1 Links 0, 1, 2, 3. Shifted when used.
	4	PEx1_[0:3]CLKn	Output	Clock Differential Lower Line for x1 Links 0, 1, 2, 3. Shifted when used.
PCIe x4	8	PEx4_[0:1]T(#)p	Output	Transmit Differential Upper Lines for the x4 Links. The x4 Links should be shifted when used.
	8	PEx4_[0:1]T(#)n	Output	Transmit Differential Lower Lines for x4 Links. The x4 Links should be shifted when used.
	8	PEx4_[0:1]R(#)p	Input	Receive Differential Upper Lines for the x4 Links. The x4 Links should be shifted when used.
	8	PEx4_[0:1]R(#)n	Input	Receive Differential Lower Lines for the x4 Links. The x4 Links should be shifted when used.
	1	PEx16_x8_x4_CLKp	Output	Clock Differential Upper Line for x16 or first x8 or x4 Link. Re-driven when used
	1	PEx16_x8_x4_CLKn	Output	Clock Differential Lower Line for x16 or first x8 or x4 Link. Re-driven when used
PCIe x16 or PCIe x8	16 16	PEx16_0T(#)p PEx8_[0:1]T(#)p	Output	Transmit Differential Upper Lines for the x16, x8 or the x4 Links. The x8 Links should be shifted when used.
	16 16	PEx16_0T(#)n PEx8_[0:1]T(#)n	Output	Transmit Differential Lower Lines for x16, x8 or the x4 Links. The x8 Links should be shifted when used.
	16 16	PEx16_0R(#)p PEx8_[0:1]R(#)p	Input	Receive Differential Upper Lines for the x16, x8, or the x4 Links. The x 8 Links should be shifted when used.
	16 16	PEx16_0R(#)n PEx8_[0:1]R(#)n	Input	Receive Differential Lower Lines for the x16, x8, or the x4 Links. The x8 Links should be shifted when used.
	1	PEx16_x8_x4_CLKp	Output	Clock Differential Upper Line for x16 or first x8 or x4 Link. Re-driven when used
	1	PEx16_x8_x4_CLKn	Output	Clock Differential Lower Line for x16 or first x8 or x4 Link. Re-driven when used
Stacking Control	1	STK0/WAKE#	Input	Stacking bit 0/Wake on LAN
	1	STK1/SDVO_DAT	In/Out	Stacking bit 1/SDVO Data
	1	STK1/PEG_ENA#	Input	Stacking bit 2/x16 Link or Alternate Function Enable
USB 2.0	2	USB_[1:0]p	Bidirectional	Differential Upper Lines for USB 2.0 Links 0, 1. Shifted when used.
	2	USB_[1:0]n		Differential Lower Lines for USB 2.0 Links 0, 1. Shifted when used.
	1	USB_OC	Input	Over-current detect for USB. Pulled low by device.
Misc.	1	DIR	Output	Direction indicates to the Device if it is installed above or below the Host
PCIe	1	PERST#	Output	Reset for PCI Express Bus
ATX Power Supply	1	PSON#	Output	Power Supply On brings the ATX power supply out of sleep mode.
	1	PWRGOOD	Input	Power Good from the power supply indicates power is good
	2	+5V_SB	Power	Standby Power for advanced power saving modes. Always on
	2	+5V	Power	+5V central power planes
	2	+3.3V	Power	+3.3V power
	1	+12V	Power	+12V central power plane
	46	GND	Power	GND pins
SMB	1	SMB_Clk	Output	Clock for SMBus
	1	SMB_Data	Bidirectional	Data for SMBus
	1	SMB_Alert#	Input	Alert for SMBus
	# indicates the lane within a link			
	[0:3] indicates link 0, 1, 2, or 3			
	[0:1] indicates link 0 or 1			

Table 2-1 shows only the required pins, arranged in functional groups, for the various buses housed in Connector A Type 1. This version of the stackable PCI Express is as defined in the *PCIe Base Specification Revision 1.1* with the exception that Hot plug present detect, Hot plug detect, and JTAG are not supported.

2.2.2 PCIe/104 Type 2

Table 2-2 Connector A Type 2 Signals

Group	Pins	Signal Name	Host Direction	Description
PCIe x1	4	PEx1_[0:3]Tp	Output	Transmit Differential Upper Line for x1 Links 0, 1, 2, 3. Shifted when used.
	4	PEx1_[0:3]Tn	Output	Transmit Differential Lower Line for x1 Links 0, 1, 2, 3. Shifted when used.
	4	PEx1_[0:3]Rp	Input	Receive Differential Upper Line for x1 Links 0, 1, 2, 3. Shifted when used.
	4	PEx1_[0:3]Rn	Input	Receive Differential Lower Line for x1 Links 0, 1, 2, 3. Shifted when used.
	4	PEx1_[0:3]CLKp	Output	Clock Differential Upper Line for x1 Links 0, 1, 2, 3. Shifted when used.
	4	PEx1_[0:3]CLKn	Output	Clock Differential Lower Line for x1 Links 0, 1, 2, 3. Shifted when used.
PCIe x4	8	PEx4_[0:1]T(#)p	Output	Transmit Differential Upper Lines for the x4 Links. The x4 Links should be shifted when used.
	8	PEx4_[0:1]T(#)n	Output	Transmit Differential Lower Lines for x4 Links. The x4 Links should be shifted when used.
	8	PEx4_[0:1]R(#)p	Input	Receive Differential Upper Lines for the x4 Links. The x4 Links should be shifted when used.
	8	PEx4_[0:1]R(#)n	Input	Receive Differential Lower Lines for the x4 Links. The x4 Links should be shifted when used.
	1	PEx16_x8_x4_CLKp	Output	Clock Differential Upper Line for x16 or first x8 or x4 Link. Re-driven when used
	1	PEx16_x8_x4_CLKn	Output	Clock Differential Lower Line for x16 or first x8 or x4 Link. Re-driven when used
SATA	4	SATA_T[0:1]p	Output	Transmit Differential Upper Line for SATA Links 0 and 1. Shifted when used.
	4	SATA_T[0:1]n	Output	Transmit Differential Lower Line for SATA Links 0 and 1. Shifted when used.
	4	SATA_R[0:1]p	Input	Receive Differential Upper Line for SATA Links 0 and 1. Shifted when used.
	4	SATA_R[0:1]n	Input	Receive Differential Lower Line for SATA Links 0 and 1. Shifted when used.
	2	SATA_DET#[0:1]	Input	Active low input to the host to indicate that a drive is attached. Only used in hot-pluggable applications. Pull up to +3.3V at the host. Ground at the device when it is attached. High impedance at the device when it is not attached, or when the drive is going to be removed. Shifted along with the other SATA signals. Optional.
	2	SATA_PWREN#[0:1]	Output	Active low output from the host to enable power to the device. Only used in hot-pluggable applications. Pull up to +3.3V at the device. Assert low at the host when the device is to be powered (i.e. in response to SATA_DET# being asserted). Shifted along with the other SATA signals. Optional.
Stacking Control	1	STK0/WAKE#	Input	Stacking bit 0/Wake on LAN
	1	STK1/SDVO_DAT	In/Out	Stacking bit 1/SDVO Data
	1	STK1/PEG_ENA#	Input	Stacking bit 2/x16 Link or Alternate Function Enable
USB 2.0	2	USB_[1:0]p	Bidirectional	Differential Upper Lines for USB 2.0 Links 0, 1. Shifted when used.
	2	USB_[1:0]n		Differential Lower Lines for USB 2.0 Links 0, 1. Shifted when used.
	1	USB_OC	Input	Over-current detect for USB. Pulled low by device.
USB 3.0	2	SSTX_[0:1]p	Output	Transmit Differential Upper Line for USB 3.0 Links 0, 1. Shifted when used.
	2	SSTX _[0:1]n	Output	Transmit Differential Lower Line for USB 3.0 Links 0, 1. Shifted when used.
	2	SSRX _[0:1]p	Input	Receive Differential Upper Line for USB 3.0 Links 0, 1. Shifted when used.
	2	SSRX _[0:1]n	Input	Receive Differential Lower Line for USB 3.0 Links 0, 1. Shifted when used.
Misc.	1	DIR	Output	Direction indicates to the Device if it is installed above or below the Host
PCIe	1	PERST#	Output	Reset for PCI Express Bus
ATX Power Supply	1	PSON#	Output	Power Supply On brings the ATX power supply out of sleep mode.
	1	PWRGOOD	Input	Power Good from the power supply indicates power is good
	2	+5V_SB	Power	Standby Power for advanced power saving modes. Always on
	2	+5V	Power	+5V central power planes
	2	+3.3V	Power	+3.3V power
	1	+12V	Power	+12V central power plane
	1	RTC_Battery	Power	Battery for real time clock (with diode, series resistor, and capacitor)
	46	GND	Power	GND pins
SMB	1	SMB_Clk	Output	Clock for SMBus
	1	SMB_Data	Bidirectional	Data for SMBus
	1	SMB_Alert#	Input	Alert for SMBus
Reserved	4	Reserved		Reserved – Do not make any connection to these pins
	# indicates the lane within a link			
	[0:3] indicates link 0, 1, 2, or 3			
	[0:1] indicates link 0 or 1			

Table 2-2 Connector A Type 2 Signals shows only the required pins, arranged in functional groups, for the various buses housed in Connector A Type 2. This version of the stackable PCI Express is as defined in the *PCIe Base Specification Revision 1.1* with the exception that Hot plug present detect, Hot plug detect, and JTAG are not supported.

2.3. Signal Naming Convention

The PCI Express signals on Connector A are named so that signal groupings are obvious. The fields in a signal name go from general to specific. The PCI Express signals start with the characters "PE," followed by the width of the Link ("x1", "x4", "x8", or "x16"), followed by an underscore "_". Next is the Link number if there is more than one Link of that width. Then is either "T", "R", or "Clk" for Transmit, Receive, or Clock respectively. Next is the lane number in the link in parenthesis, for the links that have more than one lane. Last is "p" or "n" for the positive and negative signal in the differential pair.

For example, Pex4_0T(2)p is the positive signal in lane number 2 of the first x4 Link.

A signal on the connector is designated "transmit" or "receive" in a Host-centric manner. The "transmit" pin on the Host connects to the "T" (transmit) pin of the connector. From there, the signal connects to "receive" pin of the Device.

In a PCI Express system the transmit pins of the chip are always connected to the receive pins of the other chip in the link, and vice-versa. For example, for a specific link, transmit on the Host chip is connected to receive on the Device chip, and receive on the Host is connected to transmit on the Device.

Other non-PCI Express signals follow a similar convention.

2.4. Pin Assignment

On both of these connectors, the odd-numbered pins are located towards the edge of the board, and the even numbered pins are located towards the inside of the board. Signals were assigned to pins to simplify breakout and reduce trace lengths of the PCI Express signals around Connector A. See Table 2-3 for Type 1 and Table 2-4 for Type 2 pin assignments.

Table 2-3 Connector A, Type 1 Pin Assignments

Top View Signal Assignment				
1	USB_OC#		PE_RST#	2
3	3.3V		3.3V	4
5	USB_1p		USB_0p	6
7	USB_1n		USB_0n	8
9	GND		GND	10
11	PEx1_1Tp		PEx1_0Tp	12
13	PEx1_1Tn		PEx1_0Tn	14
15	GND		GND	16
17	PEx1_2Tp		PEx1_3Tp	18
19	PEx1_2Tn		PEx1_3Tn	20
21	GND		GND	22
23	PEx1_1Rp		PEx1_0Rp	24
25	PEx1_1Rn	+5 Volts	PEx1_0Rn	26
27	GND		GND	28
29	PEx1_2Rp		PEx1_3Rp	30
31	PEx1_2Rn		PEx1_3Rn	32
33	GND		GND	34
35	PEx1_1Clkp		PEx1_0Clkp	36
37	PEx1_1Clkn		PEx1_0Clkn	38
39	+5V_SB		+5V_SB	40
41	PEx1_2Clkp		PEx1_3Clkp	42
43	PEx1_2Clkn		PEx1_3Clkn	44
45	DIR		PWRGOOD	46
47	SMB_DAT		PEx16_Clkp	48
49	SMB_CLK		PEx16_Clkn	50
51	SMB_ALERT		PSON#	52

Bank 1

Bottom View Signal Assignment				
2	PE_RST#		USB_OC#	1
4	3.3V		3.3V	3
6	USB_0p		USB_1p	5
8	USB_0n		USB_1n	7
10	GND		GND	9
12	PEx1_0Tp		PEx1_1Tp	11
14	PEx1_0Tn		PEx1_1Tn	13
16	GND		GND	15
18	PEx1_3Tp		PEx1_2Tp	17
20	PEx1_3Tn		PEx1_2Tn	19
22	GND		GND	21
24	PEx1_0Rp		PEx1_1Rp	23
26	PEx1_0Rn	+5 Volts	PEx1_1Rn	25
28	GND		GND	27
30	PEx1_3Rp		PEx1_2Rp	29
32	PEx1_3Rn		PEx1_2Rn	31
34	GND		GND	33
36	PEx1_0Clkp		PEx1_1Clkp	35
38	PEx1_0Clkn		PEx1_1Clkn	37
40	+5V_SB		+5V_SB	39
42	PEx1_3Clkp		PEx1_2Clkp	41
44	PEx1_3Clkn		PEx1_2Clkn	43
46	PWRGOOD		DIR	45
48	PEx16_Clkp		SMB_DAT	47
50	PEx16_Clkn		SMB_CLK	49
52	PSON#		SMB_ALERT	51

	4 PCIe x1
	PCIe x16
	2 USB 2.0
	1 SMB
XXX	Misc.
xxx	Pwr/Gnd

53	STK0 / WAKE#		STK1 / PEG_ENA#	54
55	GND		GND	56
57	PEx16_0T(8)p		PEx16_0T(0)p	58
59	PEx16_0T(8)n		PEx16_0T(0)n	60
61	GND		GND	62
63	PEx16_0T(9)p		PEx16_0T(1)p	64
65	PEx16_0T(9)n		PEx16_0T(1)n	66
67	GND		GND	68
69	PEx16_0T(10)p		PEx16_0T(2)p	70
71	PEx16_0T(10)n		PEx16_0T(2)n	72
73	GND		GND	74
75	PEx16_0T(11)p		PEx16_0T(3)p	76
77	PEx16_0T(11)n		PEx16_0T(3)n	78
79	GND		GND	80
81	PEx16_0T(12)p		PEx16_0T(4)p	82
83	PEx16_0T(12)n		PEx16_0T(4)n	84
85	GND		GND	86
87	PEx16_0T(13)p		PEx16_0T(5)p	88
89	PEx16_0T(13)n		PEx16_0T(5)n	90
91	GND		GND	92
93	PEx16_0T(14)p		PEx16_0T(6)p	94
95	PEx16_0T(14)n		PEx16_0T(6)n	96
97	GND		GND	98
99	PEx16_0T(15)p		PEx16_0T(7)p	100
101	PEx16_0T(15)n		PEx16_0T(7)n	102
103	GND		GND	104

Toward edge of board | +5 Volts | Toward center of board | Bank 2

54	STK1 / PEG_ENA#		STK0 / WAKE#	53
56	GND		GND	55
58	PEx16_0T(0)p		PEx16_0T(8)p	57
60	PEx16_0T(0)n		PEx16_0T(8)n	59
62	GND		GND	61
64	PEx16_0T(1)p		PEx16_0T(9)p	63
66	PEx16_0T(1)n		PEx16_0T(9)n	65
68	GND		GND	67
70	PEx16_0T(2)p		PEx16_0T(10)p	69
72	PEx16_0T(2)n		PEx16_0T(10)n	71
74	GND		GND	73
76	PEx16_0T(3)p		PEx16_0T(11)p	75
78	PEx16_0T(3)n		PEx16_0T(11)n	77
80	GND		GND	79
82	PEx16_0T(4)p		PEx16_0T(12)p	81
84	PEx16_0T(4)n		PEx16_0T(12)n	83
86	GND		GND	85
88	PEx16_0T(5)p		PEx16_0T(13)p	87
90	PEx16_0T(5)n		PEx16_0T(13)n	89
92	GND		GND	91
94	PEx16_0T(6)p		PEx16_0T(14)p	93
96	PEx16_0T(6)n		PEx16_0T(14)n	95
98	GND		GND	97
100	PEx16_0T(7)p		PEx16_0T(15)p	99
102	PEx16_0T(7)n		PEx16_0T(15)n	101
104	GND		GND	103

Toward center of board | +5 Volts | Toward edge of board

105	STK2 / SDVO_DAT		SDVO_CLK	106
107	GND		GND	108
109	PEx16_0R(8)p		PEx16_0R(0)p	110
111	PEx16_0R(8)n		PEx16_0R(0)n	112
113	GND		GND	114
115	PEx16_0R(9)p		PEx16_0R(1)p	116
117	PEx16_0R(9)n		PEx16_0R(1)n	118
119	GND		GND	120
121	PEx16_0R(10)p		PEx16_0R(2)p	122
123	PEx16_0R(10)n		PEx16_0R(2)n	124
125	GND		GND	126
127	PEx16_0R(11)p		PEx16_0R(3)p	128
129	PEx16_0R(11)n		PEx16_0R(3)n	130
131	GND		GND	132
133	PEx16_0R(12)p		PEx16_0R(4)p	134
135	PEx16_0R(12)n		PEx16_0R(4)n	136
137	GND		GND	138
139	PEx16_0R(13)p		PEx16_0R(5)p	140
141	PEx16_0R(13)n		PEx16_0R(5)n	142
143	GND		GND	144
145	PEx16_0R(14)p		PEx16_0R(6)p	146
147	PEx16_0R(14)n		PEx16_0R(6)n	148
149	GND		GND	150
151	PEx16_0R(15)p		PEx16_0R(7)p	152
153	PEx16_0R(15)n		PEx16_0R(7)n	154
155	GND		GND	156

+12 Volts | Bank 3

106	SDVO_CLK		STK2 / SDVO_DAT	105
108	GND		GND	107
110	PEx16_0R(0)p		PEx16_0R(8)p	109
112	PEx16_0R(0)n		PEx16_0R(8)n	111
114	GND		GND	113
116	PEx16_0R(1)p		PEx16_0R(9)p	115
118	PEx16_0R(1)n		PEx16_0R(9)n	117
120	GND		GND	119
122	PEx16_0R(2)p		PEx16_0R(10)p	121
124	PEx16_0R(2)n		PEx16_0R(10)n	123
126	GND		GND	125
128	PEx16_0R(3)p		PEx16_0R(11)p	127
130	PEx16_0R(3)n		PEx16_0R(11)n	129
132	GND		GND	131
134	PEx16_0R(4)p		PEx16_0R(12)p	133
136	PEx16_0R(4)n		PEx16_0R(12)n	135
138	GND		GND	137
140	PEx16_0R(5)p		PEx16_0R(13)p	139
142	PEx16_0R(5)n		PEx16_0R(13)n	141
144	GND		GND	143
146	PEx16_0R(6)p		PEx16_0R(14)p	145
148	PEx16_0R(6)n		PEx16_0R(14)n	147
150	GND		GND	149
152	PEx16_0R(7)p		PEx16_0R(15)p	151
154	PEx16_0R(7)n		PEx16_0R(15)n	153
156	GND		GND	155

Table 2-4 Connector A, Type 2 Pin Assignments

Top View Signal Assignment					Bottom View Signal Assignment				
1	USB_OC#	+5 Volts	PE_RST#	2	2	PE_RST#	+5 Volts	USB_OC#	1
3	3.3V		3.3V	4	4	3.3V		3.3V	3
5	USB_1p		USB_0p	6	6	USB_0p		USB_1p	5
7	USB_1n		USB_0n	8	8	USB_0n		USB_1n	7
9	GND		GND	10	10	GND		GND	9
11	PEx1_1Tp		PEx1_0Tp	12	12	PEx1_0Tp		PEx1_1Tp	11
13	PEx1_1Tn		PEx1_0Tn	14	14	PEx1_0Tn		PEx1_1Tn	13
15	GND		GND	16	16	GND		GND	15
17	PEx1_2Tp		PEx1_3Tp	18	18	PEx1_3Tp		PEx1_2Tp	17
19	PEx1_2Tn		PEx1_3Tn	20	20	PEx1_3Tn		PEx1_2Tn	19
21	GND		GND	22	22	GND		GND	21
23	PEx1_1Rp		PEx1_0Rp	24	24	PEx1_0Rp		PEx1_1Rp	23
25	PEx1_1Rn		PEx1_0Rn	26	26	PEx1_0Rn		PEx1_1Rn	25
27	GND		GND	28	28	GND		GND	27
29	PEx1_2Rp		PEx1_3Rp	30	30	PEx1_3Rp		PEx1_2Rp	29
31	PEx1_2Rn		PEx1_3Rn	32	32	PEx1_3Rn		PEx1_2Rn	31
33	GND		GND	34	34	GND		GND	33
35	PEx1_1Clkp		PEx1_0Clkp	36	36	PEx1_0Clkp		PEx1_1Clkp	35
37	PEx1_1Clkn		PEx1_0Clkn	38	38	PEx1_0Clkn		PEx1_1Clkn	37
39	+5V_SB		+5V_SB	40	40	+5V_SB		+5V_SB	39
41	PEx1_2Clkp		PEx1_3Clkp	42	42	PEx1_3Clkp		PEx1_2Clkp	41
43	PEx1_2Clkn		PEx1_3Clkn	44	44	PEx1_3Clkn		PEx1_2Clkn	43
45	DIR		PWRGOOD	46	46	PWRGOOD		DIR	45
47	SMB_DAT		PEx_x4_Clkp	48	48	PEx_x4_Clkp		SMB_DAT	47
49	SMB_CLK		PEx_x4_Clkn	50	50	PEx_x4_Clkn		SMB_CLK	49
51	SMB_ALERT		PSON#	52	52	PSON#		SMB_ALERT	51
				Bank 1					
53	STK0 / WAKE#	+5 Volts	STK1 / PEG_ENA#	54	54	STK1 / PEG_ENA#	+5 Volts	STK0 / WAKE#	53
55	GND		GND	56	56	GND		GND	55
57	PEx4_1T(0)p		PEx4_0T(0)p	58	58	PEx4_0T(0)p		PEx4_1T(0)p	57
59	PEx4_1T(0)n		PEx4_0T(0)n	60	60	PEx4_0T(0)n		PEx4_1T(0)n	59
61	GND		GND	62	62	GND		GND	61
63	PEx4_1T(1)p		PEx4_0T(1)p	64	64	PEx4_0T(1)p		PEx4_1T(1)p	63
65	PEx4_1T(1)n		PEx4_0T(1)n	66	66	PEx4_0T(1)n		PEx4_1T(1)n	65
67	GND		GND	68	68	GND		GND	67
69	PEx4_1T(2)p		PEx4_0T(2)p	70	70	PEx4_0T(2)p		PEx4_1T(2)p	69
71	PEx4_1T(2)n		PEx4_0T(2)n	72	72	PEx4_0T(2)n		PEx4_1T(2)n	71
73	GND		GND	74	74	GND		GND	73
75	PEx4_1T(3)p		PEx4_0T(3)p	76	76	PEx4_0T(3)p		PEx4_1T(3)p	75
77	PEx4_1T(3)n		PEx4_0T(3)n	78	78	PEx4_0T(3)n		PEx4_1T(3)n	77
79	GND		GND	80	80	GND		GND	79
81	SATA_T1p		SATA_T0p	82	82	SATA_T0p		SATA_T1p	81
83	SATA_T1n		SATA_T0n	84	84	SATA_T0n		SATA_T1n	83
85	GND		GND	86	86	GND		GND	85
87	SSTX1p		SSTX0p	88	88	SSTX0p		SSTX1p	87
89	SSTX1n		SSTX0n	90	90	SSTX0n		SSTX1n	89
91	GND		GND	92	92	GND		GND	91
93	*Reserved*		*Reserved*	94	94	*Reserved*		*Reserved*	93
95	*Reserved*		*Reserved*	96	96	*Reserved*		*Reserved*	95
97	GND		GND	98	98	GND		GND	97
99	*SATA_DET#1*		*SATA_DET#0*	100	100	*SATA_DET#0*		*SATA_DET#1*	99
101	*SATA_PWREN#1*		*SATA_PWREN#0*	102	102	*SATA_PWREN#0*		*SATA_PWREN#1*	101
103	GND		GND	104	104	GND		GND	103
				Bank 2					
105	STK2 / SDVO_DAT	+12 Volts	LPC_CLK	106	106	LPC_CLK	+12 Volts	STK2 / SDVO_DAT	105
107	GND		GND	108	108	GND		GND	107
109	PEx4_1R(0)p		PEx4_0R(0)p	110	110	PEx4_0R(0)p		PEx4_1R(0)p	109
111	PEx4_1R(0)n		PEx4_0R(0)n	112	112	PEx4_0R(0)n		PEx4_1R(0)n	111
113	GND		GND	114	114	GND		GND	113
115	PEx4_1R(1)p		PEx4_0R(1)p	116	116	PEx4_0R(1)p		PEx4_1R(1)p	115
117	PEx4_1R(1)n		PEx4_0R(1)n	118	118	PEx4_0R(1)n		PEx4_1R(1)n	117
119	GND		GND	120	120	GND		GND	119
121	PEx4_1R(2)p		PEx4_0R(2)p	122	122	PEx4_0R(2)p		PEx4_1R(2)p	121
123	PEx4_1R(2)n		PEx4_0R(2)n	124	124	PEx4_0R(2)n		PEx4_1R(2)n	123
125	GND		GND	126	126	GND		GND	125
127	PEx4_1R(3)p		PEx4_0R(3)p	128	128	PEx4_0R(3)p		PEx4_1R(3)p	127
129	PEx4_1R(3)n		PEx4_0R(3)n	130	130	PEx4_0R(3)n		PEx4_1R(3)n	129
131	GND		GND	132	132	GND		GND	131
133	SATA_R1p		SATA_R0p	134	134	SATA_R0p		SATA_R1p	133
135	SATA_R1n		SATA_R0n	136	136	SATA_R0n		SATA_R1n	135
137	GND		GND	138	138	GND		GND	137
139	SSRX1p		SSRX0p	140	140	SSRX0p		SSRX1p	139
141	SSRX1n		SSRX0n	142	142	SSRX0n		SSRX1n	141
143	GND		GND	144	144	GND		GND	143
145	LPC_AD0		LPC_DRQ#	146	146	LPC_DRQ#		LPC_AD0	145
147	LPC_AD1		LPC_SERIRQ#	148	148	LPC_SERIRQ#		LPC_AD1	147
149	GND		GND	150	150	GND		GND	149
151	LPC_AD2		LPC_FRAME#	152	152	LPC_FRAME#		LPC_AD2	151
153	LPC_AD3		*RTC_Battery*	154	154	*RTC_Battery*		LPC_AD3	153
155	GND		GND	156	156	GND		GND	155
				Bank 3					

Toward edge of board

Toward center of board

Toward center of board

Toward edge of board

	4 PCIe x1
	2 PCIe x4
	2 USB 2.0
	2 USB 3.0
	2 SATA
	1 LPC
	1 SMB
XXX	Misc.
xxx	Pwr/Gnd

2.4.1 Type 1 x16 PCI Express Link

Type 1 connector banks 2 and 3 provide an x16 PCI Express link. The x16 Link allows maximum flexibility, configurability, and expandability for current and future designs. Some examples of x16 Link application are next generation graphics chips, 1/10 gigabit Ethernet chips, or use with a PCI Express Switch which can then branch the high throughput out into any number of various size Links including multiple x16 Link graphics engines. The only limitation is the bandwidth requirement for each of the branched links.

The specification allows the x16 Link on a Type 1 PCIe/104 to be configured for alternate PCI Express configurations. These include two x8 Links, two x4 Links, or an Alternate Function defined by the CPU/chipset. These alternate configurations are Host and Device dependent. A Host that supports an x16 Link is not required to support an Alternate Function, two x8, or two x4 Links. Also, a device that supports operation at x16 is not required to support operation at x8 or x4.

2.4.1.1 Two x8 or x4 Links

Two x8 or two x4 PCI Express links can be provided on the x16 Link connectors pins. When a Device uses one of the Links, the other Link is shifted according to the same rules as the x1 Links. With host support, each x8 Link may also be used as an x4 Link.

Because there is only one clock provided for the x16 Link and potentially two devices when operating as x8 or x4, any Device that operates at x8 or x4 must re-drive the clock. The clock must not incur more than 10ns of phase delay when it is re-driven.

The pin assignments for the x8 and x4 Links are shown in Table 2-5 below.

Table 2-5: x16 Link as Two x8 or Two x4 Links Top Connector

Host Transmit Signals			Host Receive Signals		
x16 Signal	**x8 Signal**	**x4 Signal**	**x16 Signal**	**x8 Signal**	**x4 Signal**
PEx16_0T(0)	PEx8_0T(0)	PEx4_0T(0)	PEx16_0R(0)	PEx8_0R(0)	PEx4_0R(0)
PEx16_0T(1)	PEx8_0T(1)	PEx4_0T(1)	PEx16_0R(1)	PEx8_0R(1)	PEx4_0R(1)
PEx16_0T(2)	PEx8_0T(2)	PEx4_0T(2)	PEx16_0R(2)	PEx8_0R(2)	PEx4_0R(2)
PEx16_0T(3)	PEx8_0T(3)	PEx4_0T(3)	PEx16_0R(3)	PEx8_0R(3)	PEx4_0R(3)
PEx16_0T(4)	PEx8_0T(4)		PEx16_0R(4)	PEx8_0R(4)	
PEx16_0T(5)	PEx8_0T(5)		PEx16_0R(5)	PEx8_0R(5)	
PEx16_0T(6)	PEx8_0T(6)		PEx16_0R(6)	PEx8_0R(6)	
PEx16_0T(7)	PEx8_0T(7)		PEx16_0R(7)	PEx8_0R(7)	
PEx16_0T(8)	PEx8_1T(0)	PEx4_1T(0)	PEx16_0R(8)	PEx8_1R(0)	PEx4_1R(0)
PEx16_0T(9)	PEx8_1T(1)	PEx4_1T(1)	PEx16_0R(9)	PEx8_1R(1)	PEx4_1R(1)
PEx16_0T(10)	PEx8_1T(2)	PEx4_1T(2)	PEx16_0R(10)	PEx8_1R(2)	PEx4_1R(2)
PEx16_0T(11)	PEx8_1T(3)	PEx4_1T(3)	PEx16_0R(11)	PEx8_1R(3)	PEx4_1R(3)
PEx16_0T(12)	PEx8_1T(4)		PEx16_0R(12)	PEx8_1R(4)	
PEx16_0T(13)	PEx8_1T(5)		PEx16_0R(13)	PEx8_1R(5)	
PEx16_0T(14)	PEx8_1T(6)		PEx16_0R(14)	PEx8_1R(6)	
PEx16_0T(15)	PEx8_1T(7)		PEx16_0R(15)	PEx8_1R(7)	

Table 2-6: x16 Link as Two x8 or Two x4 Links Bottom Connector

Host Transmit Signals			Host Receive Signals		
x16 Signal	**x8 Signal**	**x4 Signal**	**x16 Signal**	**x8 Signal**	**x4 Signal**
PEx16_0T(0)	PEx8_1T(0)	PEx4_1T(0)	PEx16_0R(0)	PEx8_1R(0)	PEx4_1R(0)
PEx16_0T(1)	PEx8_1T(1)	PEx4_1T(1)	PEx16_0R(1)	PEx8_1R(1)	PEx4_1R(1)
PEx16_0T(2)	PEx8_1T(2)	PEx4_1T(2)	PEx16_0R(2)	PEx8_1R(2)	PEx4_1R(2)
PEx16_0T(3)	PEx8_1T(3)	PEx4_1T(3)	PEx16_0R(3)	PEx8_1R(3)	PEx4_1R(3)
PEx16_0T(4)	PEx8_1T(4)		PEx16_0R(4)	PEx8_1R(4)	
PEx16_0T(5)	PEx8_1T(5)		PEx16_0R(5)	PEx8_1R(5)	
PEx16_0T(6)	PEx8_1T(6)		PEx16_0R(6)	PEx8_1R(6)	
PEx16_0T(7)	PEx8_1T(7)		PEx16_0R(7)	PEx8_1R(7)	
PEx16_0T(8)	PEx8_0T(0)	PEx4_0T(0)	PEx16_0R(8)	PEx8_0R(0)	PEx4_0R(0)
PEx16_0T(9)	PEx8_0T(1)	PEx4_0T(1)	PEx16_0R(9)	PEx8_0R(1)	PEx4_0R(1)
PEx16_0T(10)	PEx8_0T(2)	PEx4_0T(2)	PEx16_0R(10)	PEx8_0R(2)	PEx4_0R(2)
PEx16_0T(11)	PEx8_0T(3)	PEx4_0T(3)	PEx16_0R(11)	PEx8_0R(3)	PEx4_0R(3)
PEx16_0T(12)	PEx8_0T(4)		PEx16_0R(12)	PEx8_0R(4)	
PEx16_0T(13)	PEx8_0T(5)		PEx16_0R(13)	PEx8_0R(5)	
PEx16_0T(14)	PEx8_0T(6)		PEx16_0R(14)	PEx8_0R(6)	
PEx16_0T(15)	PEx8_0T(7)		PEx16_0R(15)	PEx8_0R(7)	

2.4.2 PEG_ENA# Signal

The PEG_ENA# signal is used to indicate the presence of a device on the x16 Link. This signal is pulled up at the Host. Any Device that uses the x16 Link (or the x16 as an x8 or x4) attaches this signal to ground. When the Host sees this signal high, indicating that an x16 Device is not present, it may disable the x16 Link, or convert it to alternate uses, such as Alternate Functions as defined by the CPU/chipset.

2.4.3 DIR Signal

The DIR line provides a means for the Devices to select the correct Link depending if it is above or below the Host in the stack.

2.4.3.1 DIR Line on Host

The state of the DIR line is always determined by the Host so that the Devices can be designed without regards to the design of other Devices. On the top side connector this line must be tied to ground on the Host. On the bottom side connector the DIR line must be tied to +5 volt power during all implemented power saving modes except power completely off. A Host that supports suspend modes may want to use +5V_Aux diode Ored with +5V in case the power supply does not provide +5V_Aux. Shown in Figure 2-1 is the required PCB connection for the DIR line on the Host.

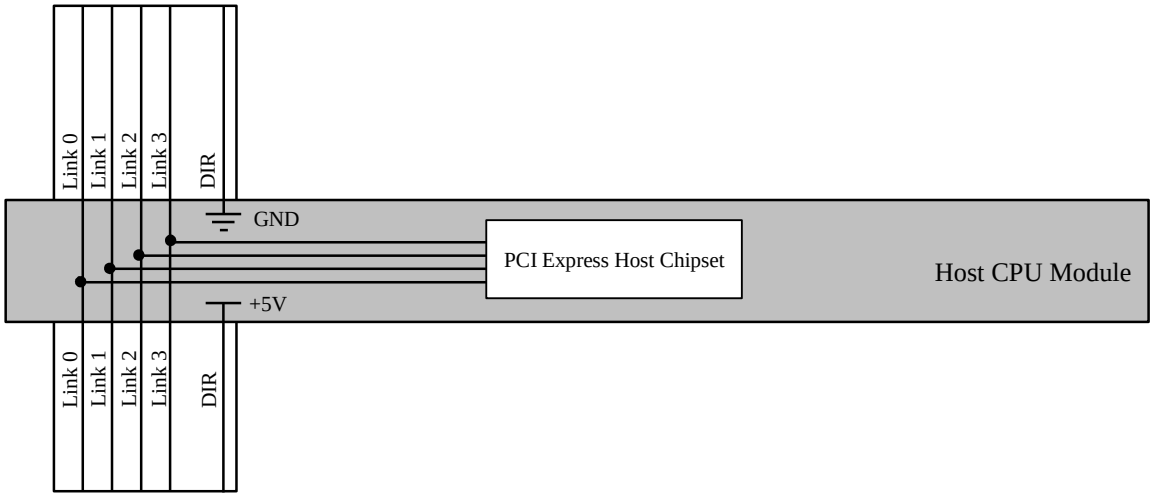


Figure 2-1 Required Circuitry for a Host Module Configuration for Automatic Link Shifting

2.4.3.2 DIR Line on Device

On the Device the DIR line is an input to the resident auto-switching multiplexers. A resistor divider is required on the DIR line on each Device to adjust the SELECT line voltage for the switches. Each Device must sink or source less than 300uA of current. Therefore, the divider resistors R1 and R2 shown in Figure 2-2 must total 15K or greater.

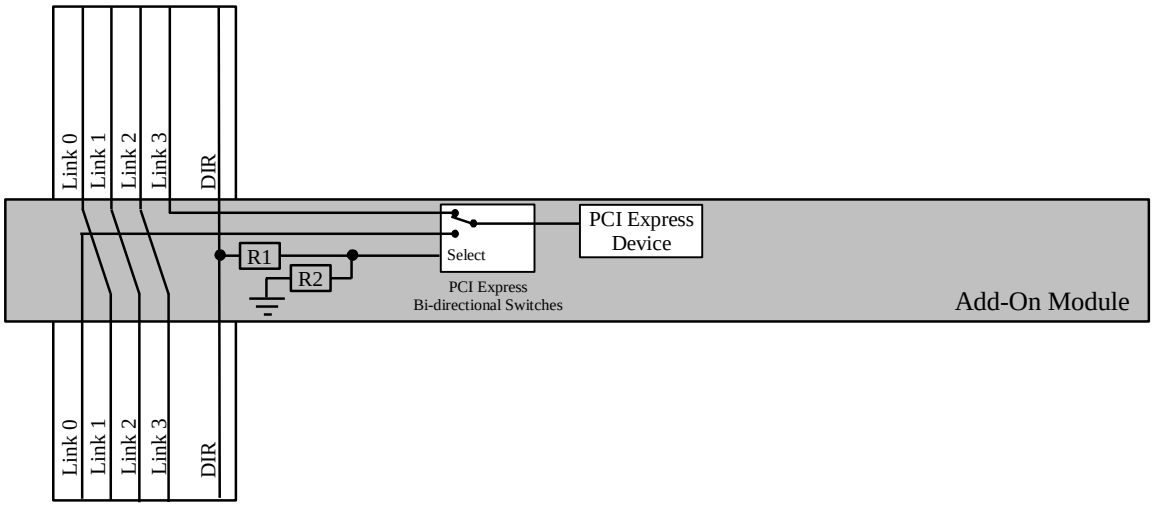


Figure 2-2 Required Device Circuitry for Automatic Link Shifting

If the Device is positioned above the Host, then the DIR signal would be grounded and the SELECT line of the multiplexers would allow Link 0 to connect to the PCI device. Links 1, 2, and 3 are then allowed to shift and pass over so that Link 1 is in the Link 0 position, Link 2 is in the Link 1 position, and Link 3 is in the Link 2 position. A left-most Link is now available for the next Device card to be stacked above the first Device.

If the Device is stacked below the module, then the DIR line would be set to +5V and the SELECT line of the multiplexers would allow Link 3 to connect to the PCI device. Links 0, 1, and 2 are then allowed to shift and pass

over so that Link 2 is in the Link 3 position, Link 1 is in the Link 2 position, and Link 0 is in the Link 1 position. A right-most link is now available for the next Device card to be stacked below the first Device.

All Devices can be built using the same methodology as a single configuration. The Links used will always be the left most links or the rights most links depending if the Device gets stacked above or below the Host.Stack-UP or Stack-DOWN Link Shifting

Within the different connector types and configurations, Connector A contains differential Link Groups. These include x1/x4/x8 PCI Express, USB 2.0, USB 3.0, and SATA. Within each group are individual point-to-point links which must be automatically shifted if one or more links out of that group are used on a Device. The x16 PCI Express, LPC, SMB, power, and control signals do not require Link shifting.

Link shifting is utilized so that Devices can be built uniformly and consistently while using dedicated point-to-point connections. Without link shifting, Devices would have to be made with a specific link identified. This would then require each Device to have multiple configurations, one for each link position. Link shifting at the PCB level allows each Device to have only one universal configuration.

In addition to automatic Link shifting, highly embedded systems require that Devices be allowed to stack above or below the Host. The key to this capability is the ability for the Devices to use either the first links or the last links depending on whether the module is above or below the Host. The DIR line tells the Device its position relative to the Host.

Note: If the host has both the top and bottom of Connector A connected devices should not be stacked above and below the Host at the same time in order to avoid signal integrity degradation due to signal path stubs.

2.4.4 PCB Link Shifting

As a demonstration of link shifting in the presence of multiple link groups, the x1 PCI Express, x4 PCI Express, USB 2.0, USB 3.0, and SATA link groups are used in Figure 2-3: Automatic Link Shifting Examples for Host and Various Devices. Any Device may use one or more Links from any group. If multiple Links are used then the necessary link shifting must be implemented on the Device PCB for each Link and Link Group. For example, in the case where two x1 Link devices are resident on the Device, it is required that the remaining two unused Links be shifted two locations in order that other Devices be able to use the remaining Links. It is not enough to shift only one link space as in the case of a one x1 Link Device.

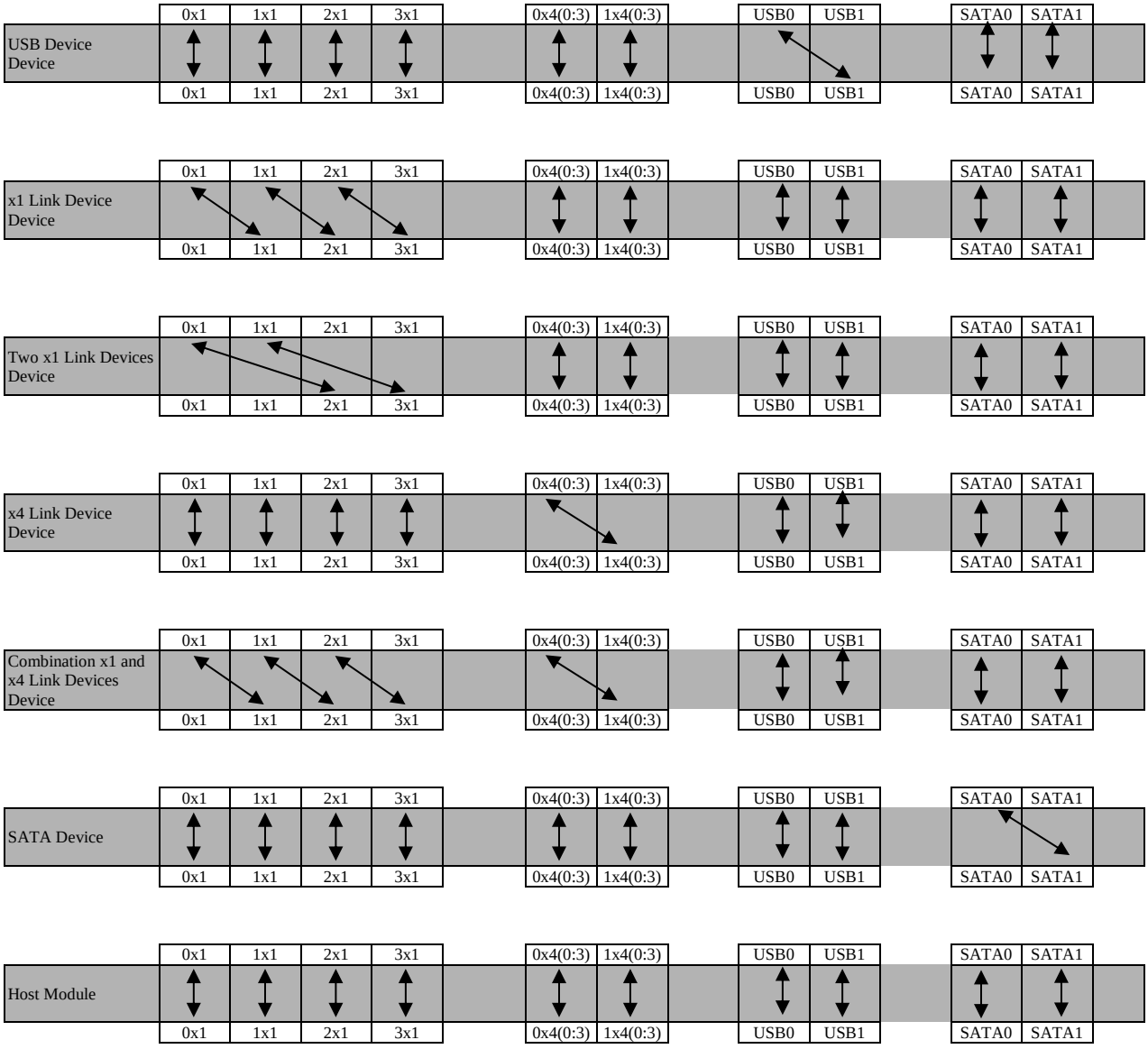


Figure 2-3: Automatic Link Shifting Examples for Host and Various Devices

2.4.5 Link Shifting Stack Examples

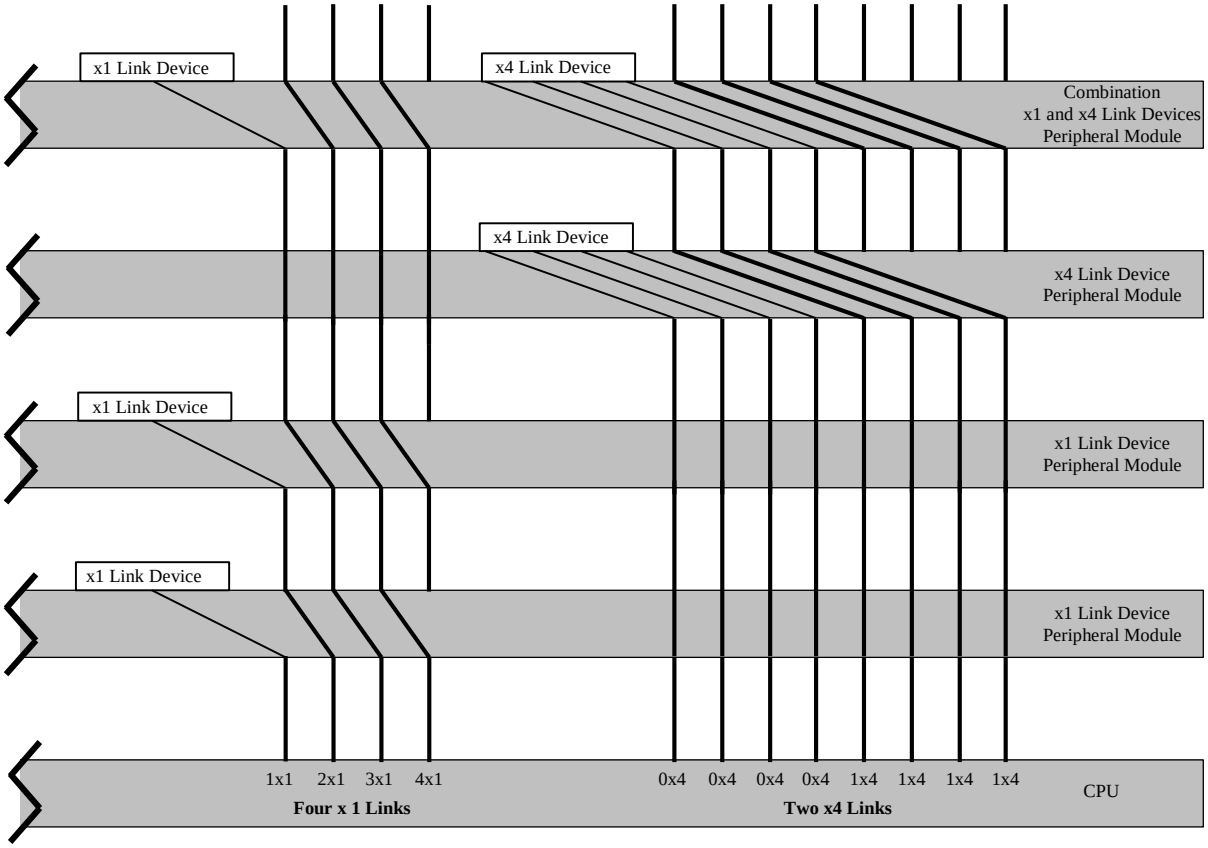


Figure 2-4: Automatic Link Shifting Stack-Up Example Consisting of Two x1 Link Device, One x4 Link Device, and One Device with One x1 Link and One x4 Link

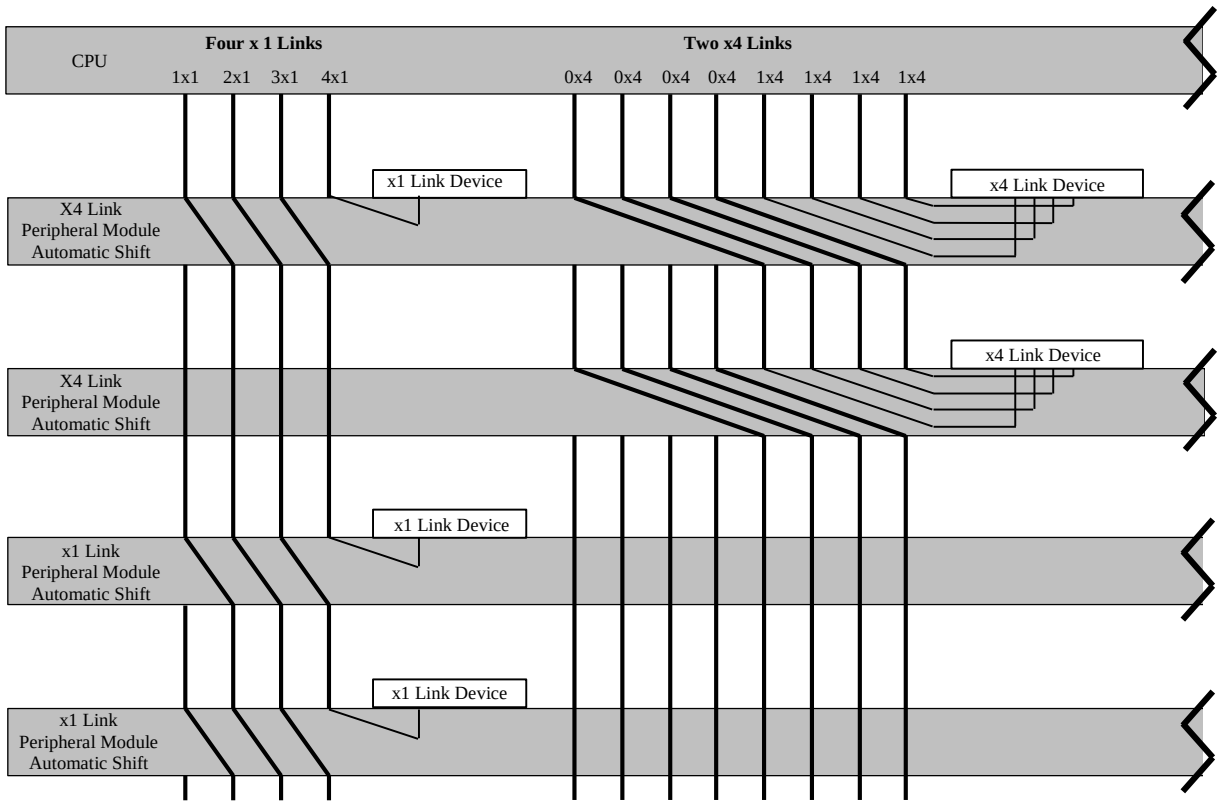


Figure 2-5: Automatic Link Shifting Stack-Down Example Consisting of Two x1 Link Device, One x4 Link Device, and One Device with One x1 Link and One x4 Link

2.5. Switching

To ensure that all Device modules can be stacked up or down without manual configuration a signal switch is required on the Device. The switch is only required on interface being used. For example a SATA Device will have a switch on the SATA link, but will not have switches on USB 3.0 or PCI Express links.

2.5.1 Signal Switch

A signal switch is an analog multiplexer that can be used to select between the link on top connector or the bottom connector. This switch must be able to perform well at the high data rates found in the PCI Express, SATA, or USB 3.0 signaling environment.

Several initial candidates for signal switches have been identified and listed in Table 2-7. These switches have advertised specifications that meet the requirements of the application but have not been independently verified. Equivalent substitutes are permitted.

Table 2-7: Signal Switches or equivalent

Manufacturer	Part Number	Application
Texas Instruments	TS2PCIE2212	PCIe 1
Pericom	PI2PCIE2442	PCIe 1
Texas Instruments	DS25MB100	PCIe 1
NXP	CBTU0808EE/G	PCIe 1
Pericom	PI2PCIE2442	PCIe 2
Maxim	MAX4889A	PCIe 2
Pericom	PI3PCIE3412	PCIe 3
Pericom	PI2USB3212	USB 3.0
Pericom	PI2DBS212	SATA 3
NXP	CBTU04083	PCIe 3, SATA 6 or USB 3.0

2.6. System Clocking

The PCI Express architecture is based on a 100 MHz reference clock that is distributed from the Host to the Devices.

The Host may employ spread spectrum clocking as defined in the PCI Express Base Specification to reduce EMI. For this reason it is recommended that Devices always use the distributed clock as its reference clock. Using an on-board oscillator as a reference is not allowed.

PCIe/104 does not provide for any termination on unused clock lines, therefore the Host is required to disable any unused clocks.

Because there is only one clock provided for the Type 1 PCI Express x16 Link or the Type 2 PCI Express x4 links and potentially two devices, any Device that operates at x8 or x4 must re-drive the clock. The clock must not incur more than 10ns of phase delay when it is re-driven.

2.7. Layout Recommendations

The Data rate for PCI Express Generation 1 is 2.5 Gbps, Generation 2 is 5.0 Gbps, and Generation 3 is 8.0 Gbps. This means that significant frequency content exists up to 1.25 GHz for Generation 1, 2.50 GHz for Generation 2, and 4.0GHz for Generation 3. At these speeds, PCB layout becomes very critical. Therefore, the following recommendations should be followed to avoid signal integrity problems:

- Route all PCI Express signal lines (Transmit and Receive) as controlled impedance using microstrip, stripline, or similar techniques.
    - 68 – 105Ω differential pairs, 85Ω recommended.
- Spacing from a link to its neighbor must be at least 20 mils (0.51 mm) in the main routing region, 15 mils (0.38 mm) for stripline breakout, and 12 mils (0.30 mm) for microstrip breakout.

- Symmetrical routing must be used between the two signals of a differential pair.
- Signals in a differential pair must be matched to within 5 mils (0.13 mm).
- AC coupling capacitors must be provided on the TX lines. Values should be between 75nF and 200nF. A surface mount capacitor must be used.
- All PCI Express signals should be routed in an adjacent layer to a ground plane.
- There shall be no stubs except the short stub caused by the unused end of the Host connector. SI testing has shown this very short stub to be insignificant in a system with a Host and 6 add-in cards. No stubs are recommended on the Host at Gen 2.
- Do not use 90 degree bends. Use 45 degree bends or curves.

Table 2-8: Via and Trace Length Budget

Location	Max. Vias	Max. Trace Length mil (mm)	Notes
Host TX lines Gen 1 & 2	4	6000 (152.40)	Both sides of AC capacitor
Host TX lines Gen 3	4	4000 (101.60)	Both sides of AC capacitor
Host RX lines Gen 1 & 2	2	6000 (152.40)	
Host RX lines Gen 3	2	4000 (101.60)	
Device TX Lines	4	4000 (101.60)	Both sides of signal switch.
Device RX lines	4	4000 (101.60)	Both sides of signal switch.
Pass-through (lane shifting)	2	1000 (25.40)	Includes stack height

2.7.1 Number of PCI Express Boards in the Stack

The last PCI Express Generation 1, SATA 1 or SATA 2 peripheral in a stack shall have no more than 10 boards between it and the host. The last PCI Express Generation 2 or USB 3.0 peripheral in a stack shall have no more than 9 boards between it and the host. The last PCI Express Generation 3 or SATA 3 peripheral in a stack shall have no more than 5 boards between it and the host.

2.8. Routing Topology

2.8.1 PCI Express and USB 3.0

Figure 2-6 below shows the positioning of the DC blocking capacitor and PCIe/104 connector in relation to the Host and Device. The DC blocking capacitor is placed on the transmit signals. This will be the signals the Host drives onto the Tx bus connector's pins and the signals the Device drives onto the Rx signals of the connector. The actual position is not critical; however the position must be closely matched between the signals of a differential pair.

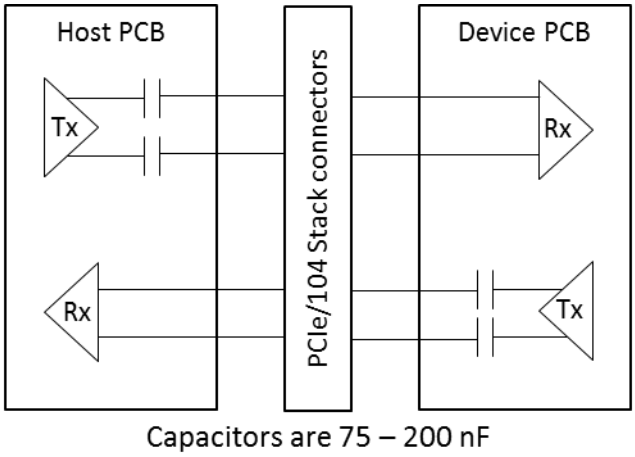


Figure 2-6 PCI Express and USB 3.0 Capacitor Placement

Table 2-9 below list the general guide lines for PCI Express routing.

Table 2-9 PCI Express and USB 3.0 Routing Specification

Interface	Differential Impedance (Ohm)	Matching in a pair mil (mm)	Matching pair to pair mil (mm)
PCIe Gen 1, 2 & 3 Capable	85 ±15%	5 (0.13)	Not required
PCIe Gen 1 only	100 ±20%	5 (0.13)	Not required
PCIe Pass Through	85 ±15%	5 (0.13)	Not required
USB 3.0	96 ±15%	N/A	N/A

2.8.2 SATA

Figure 2-7 below shows the positioning of the DC blocking capacitor and PCIe/104 connector in relation to the Host and Device. The DC blocking capacitor is placed on the transmit and receive signals. The actual position is not critical; however the position must be closely matched between the signals of a differential pair. Note that a SATA device typically has internal capacitors, if so capacitors on the PCB are not required.

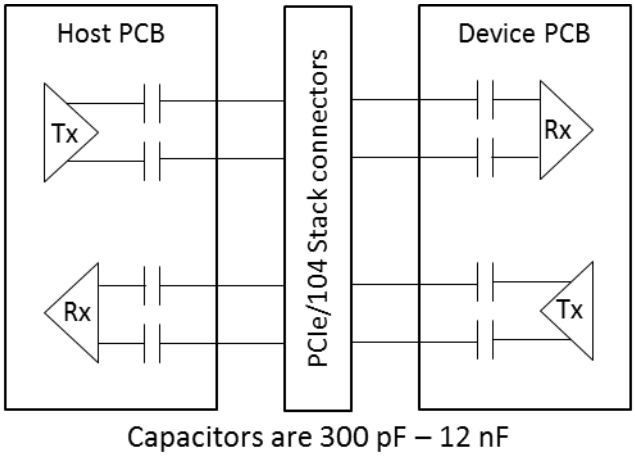


Figure 2-7 SATA Capacitor Placement

Table 2-10 below lists the general guide lines for SATA routing.

Table 2-10 SATA Routing Specification

Interface	Differential Impedance (Ohm)	Matching in a pair mil (mm)	Matching pair to pair mil (mm)
SATA	100 ±15%	N/A	N/A

2.9. Device Connector Break-out Examples

These drawings are not to scale and do not show controlled impedance lines. They are intended to show the general connections and lane shifting on a device for various PCIe/104 devices that can be stacked above or below the CPU. All power, ground, and unused signals have the top and bottom connectors connected together. The examples show the device on the top of the board; however that is not a requirement.

2.9.1 Universal PCI Express x1 Device Layout Example

Figure 2-8 below shows an example of routing a Universal x1 PCI Express link from the PCIe/104 connector to a Signal Switch. This device can be stacked either above or below the CPU and implements lane shifting.

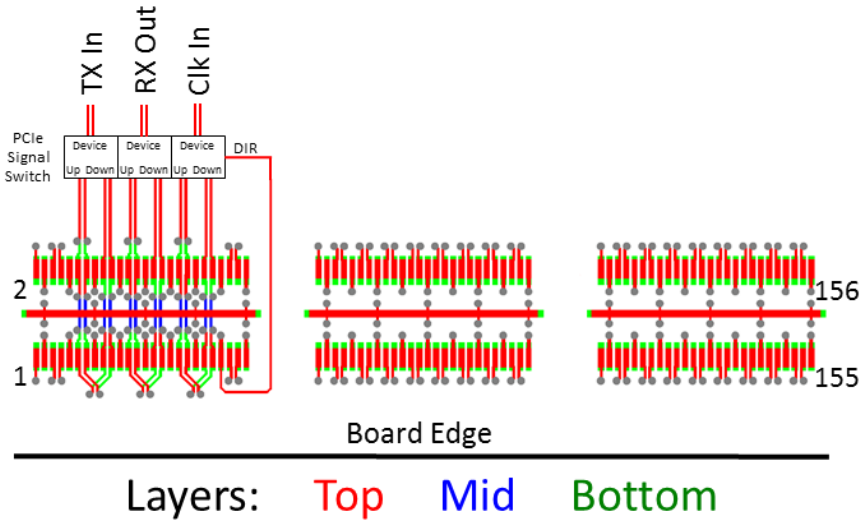


Figure 2-8 Example breakout routing of a Universal PCI Express x1 link with shifting.

2.9.2 Universal PCI Express x4 Device Layout Example

Figure 2-9 below shows an example of routing a Universal x4 PCI Express link from the PCIe/104 connector to a Signal Switch. This device can be stacked either above or below the CPU and implements lane shifting.

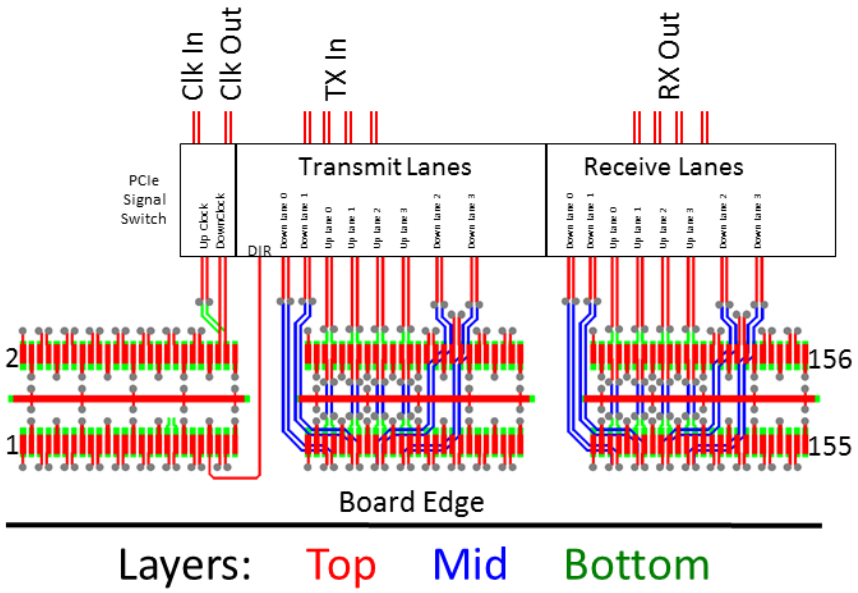


Figure 2-9 Example breakout routing a Universal PCI Express x4 link with lane shifting.

2.9.3 Type 1 PCI Express x8 Device Layout Example

Figure 2-10 below shows an example of routing a Type 1 x8 PCI Express link from the PCIe/104 connector directly to a PCI Express x8 device. This device is shown as a stack down version and implements lane shifting.

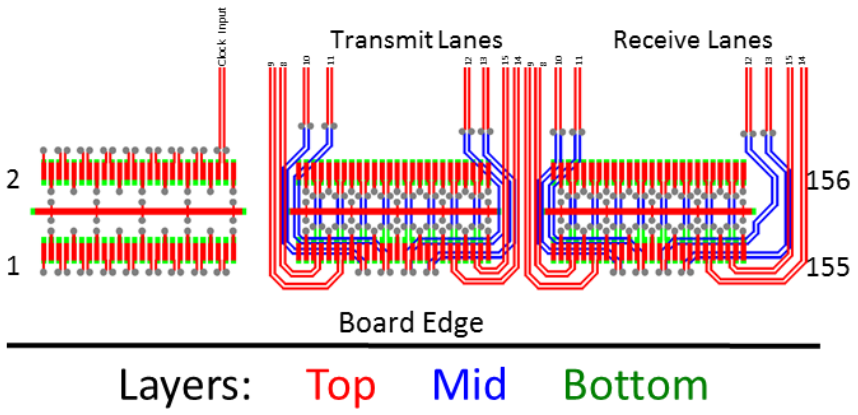


Figure 2-10 Example breakout routing a PCI Express x8 device stacking down with lane shifting.

2.9.4 Type 1 PCI Express x16 Device Layout Example

Figure 2-11 below shows an example of the routing from the Device connector directly to a PCI Express x16 device. This example is stack down and does not use lane shifting since the x16 device uses all of the lanes on the link.

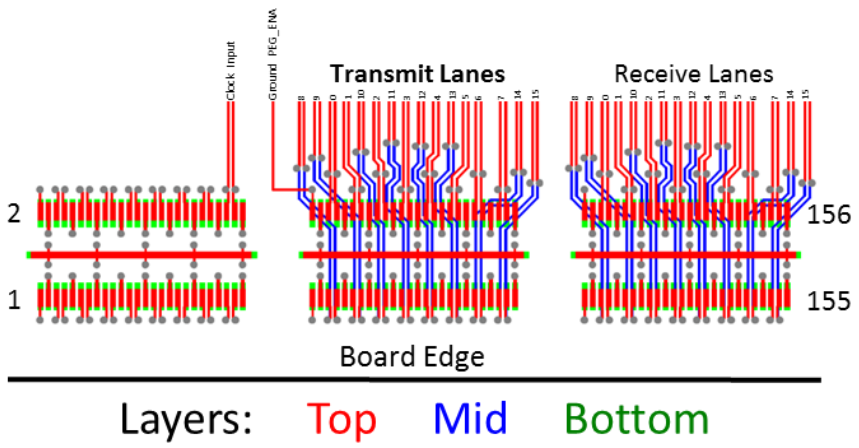


Figure 2-11 Example breakout routing a PCI Express x16 device stacking down.

2.9.5 Type 2 USB 3.0 Device Layout Example

Figure 2-12 below shows an example of routing an USB 3.0 link from the PCIe/104 connector to a Signal Switch. This device can be stacked either above or below the CPU and implements lane shifting. USB 3.0 requires that each USB 3.0 port to be associated with a USB 2.0 port as shown in this example.

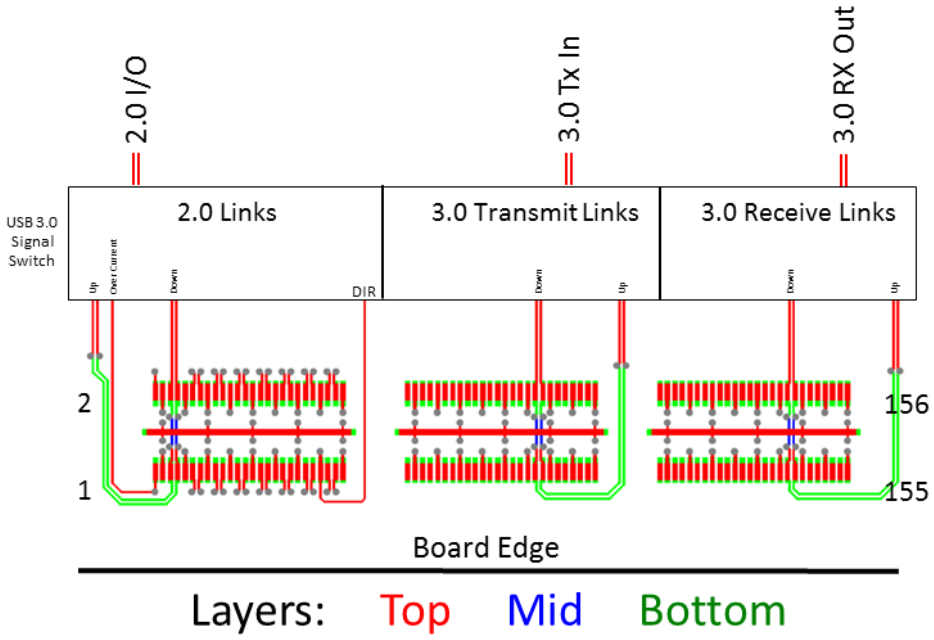


Figure 2-12 Example breakout routing an USB 3.0 device with lane shifting.

2.9.6 Type 2 SATA Device Layout Example

Figure 2-13 below shows an example of routing a SATA link from the PCIe/104 connector to a Signal Switch. This device can be stacked either above or below the CPU and implements lane shifting.

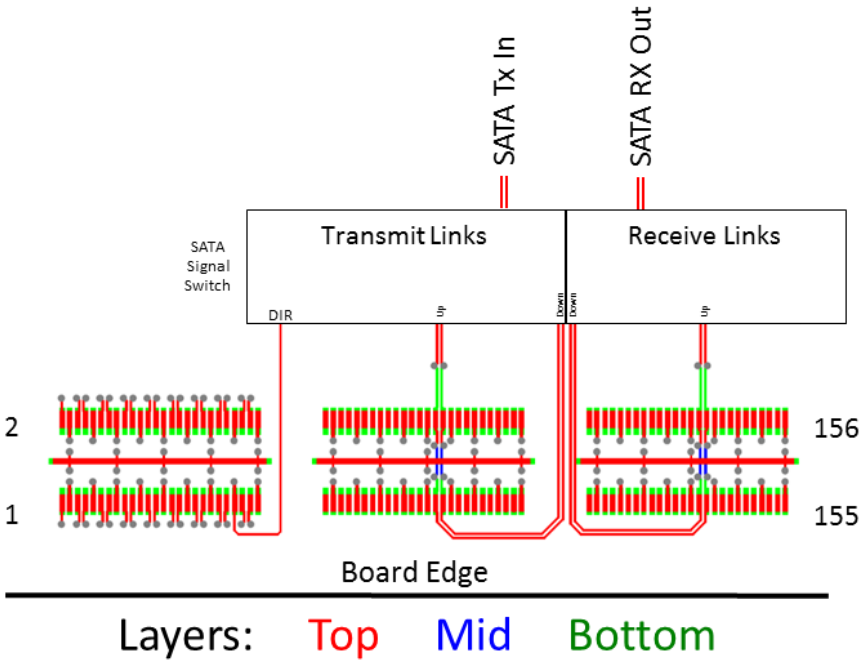


Figure 2-13 Example breakout routing a SATA device with lane shifting.

3. EXPANSION CONNECTOR B

3.1. Description

Expansion Connector B is the stackable PCI Expansion connector of the PC/104-*Plus* and PCI-104 specifications. For full details and connector location see the PC/104-*Plus* or PCI-104 Specifications published by the PC/104 Consortium

3.2. Functions

- Four 32 bit, 33 MHz PCI Bus Links each capable of Bus Mastering
- +5V_SB, PSON#, PME# for ATX power management
- Power: +3.3V, +5V, +12V, -12V

3.3. Signal Descriptions

Table 3-1 Connector B Signals

# Pins	Signal Name	Group	Description
32	AD[31:00]	PCI Bus	**Address and Data** are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases.
4	C/BE[0,3]#		**Bus Command/Byte Enables** are multiplexed. During the address phase of a transaction, they define the bus command. During the data phase, they are used as byte enables.
1	PAR		**Parity** is even parity across AD [31:00] and C/BE [3:0]#. Parity generation is required by all PCI signals.
1	FRAME#		**Cycle Frame** is driven by the current master to indicate the beginning of an access and will remain active until the final data cycle.
1	TRDY#		**Target Ready** indicates the selected device's ability to complete the current data phase of the transaction. Both IRDY# and TRDY# must be asserted to terminate a data cycle.
1	IRDY#		**Initiator Ready** indicates the bus master's ability to complete the current data phase of the transaction.
1	STOP#		**Stop** indicates the current selected device is requesting the master to stop the current transaction.
1	DEVSEL#		**Device Select**, when actively driven, indicates the driving device has decoded its address as the target of the current access.
4	IDSEL[0,3]		**Initialization Device Select** is used as a chip-select during configuration read and write transactions.
1	LOCK#		**Lock** indicates an atomic operation to a bridge that may require multiple transactions to complete.
1	PERR#		**Parity Error** is for reporting data parity errors.
1	SERR#		**System Error** is for reporting address parity errors.
4	REQ#[0,3]		**Request** indicates to the arbitrator that this device desires use of the bus.
4	GNT#[0,3]		**Grant** indicates to the requesting device that access has been granted.
4	CLK[0,3]		**Clock** provides timing for all transactions on the PCI bus and is an input to every PCI device.
1	RST#		**Reset** is used to bring PCI-specific registers, sequencers, and signals to a consistent state.
1	M66EN		**66 MHz Enable** indicates to a device whether the bus segment is operating at 33 MHz or 66 MHz. The PCI bus has been simulated at 33MHz. For the purpose of this specification, 66MHz is not supported.
1	INTA#		**Interrupt A** is used to request Interrupts.
1	INTB#		**Interrupt B** is used to request Interrupts.
1	INTC#		**Interrupt C** is used to request Interrupts.
1	INTD#		**Interrupt D** is used to request Interrupts.
1	PME#	ATX Power Supply	**Power Management Event** such as wake-on-LAN
1	+5V_SB		**Standby Power** for advanced power saving modes. Always on
1	PSON#		**Power Supply On** brings the ATX power supply out of sleep mode.
5	VI/O	Power	
10	+3.3V		**+3.3V** power lines
8	+5V		**+5V** power lines
1	+12V		**+12V** power line
1	-12V		**-12V** power line
25	GND		**Ground** lines

Table 3-1 shows only the required pins, arranged in functional groups, which are required for the stackable PCI Expansion bus. This version of the PCI bus is intended as a 32-bit bus running at 33MHz as defined in the *PCI Local Bus Specification Revision 2.2*, and therefore, 64-bit extension and 66MHz[1] are not supported at this time. Also not supported are the boundary scan features (JTAG), *Present* (PRSNT [1:2]#), and *Clock running* (CLKRUN#). The direction indication on the pins assumes a combination master/target device.

[1] The PCI bus has been simulated at 33MHz. For the purpose of this specification, 66MHz is not supported. To support future enhancements, the M66EN signal should be grounded on any module that cannot support 66MHz and left open for modules that can support a 66MHz clock.

3.4. Pin Assignment

Signals are assigned in the same relative order as in the PCI Local Bus Specification Revision 2.2, but transformed to the corresponding header connector pins. Because of the stack-through nature of the bus, slot-specific signals are duplicated for each plug-in module. The system has been designed to accommodate 4 modules, which are PC/104-*Plus*, PCI-104, or a combination of the two, so multiple sets of the signals have been duplicated to accommodate one signal for each module. These four signal groups include: IDSEL[3:0], CLK[3:0], REQ#[3:0], GNT#[3:0]. Signal assignments for the J3/P3 connector are given in Table 3-2.

Table 3-2 Connector Signal Assignment

	A	B	C	D
1	GND	+5V_SB	+5V	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1#	AD15	+3.3V
9	SERR#	GND	PSON#	PAR
10	GND	PERR#	+3.3V	PME#
11	STOP#	+3.3V	LOCK#	GND
12	+3.3V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3V
14	GND	AD16	+3.3V	C/BE2#
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VI/O
24	GND	REQ2#	+5V	GNT0#
25	GNT1#	VI/O	GNT2#	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD#	+5V	RST#
29	+12V	INTA#	INTB#	INTC#
30	-12V	REQ3#	GNT3#	GND

3.5. +5V_SB, PSON#, and PME#

To support ATX power supplies and power down features three signals have been added to the PCI bus. They are +5V_SB which is a power source that is always present when main power is supplied to the system, PSON# which is a power supple control signal that can turn the power supple on or off, and PME# which can be used to bring the CPU out of power down states such as wake-on-LAN.

These signals have been implemented on the reserved pins of the PCI expansion bus of the PC/104-*Plus* and PCI-104 Specifications at pins B1, C9, and D10. Not all manufacturers will implement these signals; therefore to maintain compatibility with existing products it is important for designs that implement these functions to protect against undriven inputs.

3.6. PCI Signaling Voltage (VI/O) Requirements

3.6.1 PCI Host Module

The PCI Host board will always determine the PCI signaling level on the bus by setting all VI/O pins to either +3.3V or +5V. If VI/O is set to 3.3V, then the system will use +3.3V I/O signaling and, likewise, if VI/O is set to +5V, then the system will use +5V I/O signaling. Some PCI host modules may only allow one of the options, while others may provide a jumper to allow the user to select the signaling level. Once the signaling level is selected, the remaining boards in the system must use that signaling level.

3.6.2 Add-In Modules

Add-in cards can be 3.3V, 5V, or universal.

3.6.2.1 3.3V Add-In Modules

3.3V add-in modules operate in environments where VI/O has been set to +3.3V by the host module. Using 5V add-in modules on a 3.3V stack will result in the 3.3V modules being damaged.

3.6.2.2 5V Add-In Modules

5V add-in modules operate in environments where VI/O has been set to +5V by the host module. Using 3.3V add-in modules on a 5V stack will result in the 3.3V modules being damaged.

3.6.2.3 Universal Add-In Modules

Universal add-in boards can be used on either 3V or 5V I/O signaling buses. Universal boards either use the VI/O signal to determine its signaling level or are 3V signaling boards that have 5V-tolerant I/O. Many PCI interface chips have a "VI/O" pin that is the power for the I/O buffers that can be directly connected to VI/O. Universal boards will work on either 3V or 5V I/O signaling buses.

4. PCIe/104 Type 1 and Type 2 Stacking

4.1. System Stacking Rules

These rules will insure that the systems are not damaged when different type peripheral boards and host modules are stacked together.

Table 4-1 Required Host State When Peripherals Are Placed on Type 1 and Type 2 Hosts

Peripheral Card		Type 1 Host Configuration				Type 2 Host
Bus Used	**Type**	**x16**	**x8**	**x4**	**Alternate Function**	
Alternate Function	1	Reset			Good	Reset
PCI Express x16	1	Good	Reset			Reset
PCI Express x8	1	Good		Reset		Reset
PCI Express x4	Universal	Good			Reset	Good
PCI Express x1	Universal	Good				Good
USB 2.0	Universal	Good				Good
USB 3.0	2	Reset				Good
SATA	2	Reset				Good
LPC	2	Reset				Good

Table 4-2 Peripheral Effect on Type 1 Host CPU Signals

Bus	Peripheral	53 STK0/WAKE#	54 STK1/PEG_ENA#	105 STK2/SDVO_DAT
Type 1	PCIe x16 or x8	No Change	0 = Enable PCIe x16	No Change
Type 1	Alternate Function	No Change	No Change	1 = Enable GFX
Type 2	SATA, USB 3.0, LPC	0 = Bus Stacking Error	No Change	No Change
Universal	PCIe x4	No Change	0 = Enable PCIe x16	No Change
Universal	PCIe x1, USB 2.0	No Change	No Change	No Change

Table 4-3 Peripheral Effect on Type 2 Host CPU Signals

Bus	Peripheral	53 STK0/WAKE#	54 STK1/PEG_ENA#	105 STK2/SDVO_DAT
Type 1	PCIe x16 or x8	No Change	0 = Bus Stacking Error	No Change
Type 1	Alternate Function	No Change	No Change	1 = Bus Stacking Error
Type 2	SATA, USB 3.0, LPC	0 = Normal Operation	No Change	No Change
Universal	PCIe x4	No Change	1 = Normal Operation	No Change
Universal	PCIe x1, USB 2.0	No Change	No Change	No Change

- The PCI Express signals may always be driven, but it is recommended that they are Hi-Z during reset.
- The system should provide some indication to the user when a bus stacking error has occurred, i.e. a blinking LED.
- A PCI Express Link may only traverse up to six stacked PCI Express connector heights and all PCI Express modules should be on the same side of the host if the top and bottom PCI Express connectors are electrically connected together.
- A PCI Express Link may only be attached to a single connector on the Host.
- A PCI bus may only traverse up to four stacked PCI connectors, and they must all be on the same side of the Host. Because of the requirements of trace length matching, all PCI Devices must be stacked together and must be next to the Host

4.2. Host Configuration Rules

There are a set of rules to ensure that improper stacking does not damage either the host or peripheral boards. In addition to connecting the pins as specified in Table 4-5, if a bus stacking error is detected the host shall hold the system in reset. The host can optionally indicate to the user a stacking error.

The signals that need special consideration are: SATA_T[0:3]n, SATA_T[0:3]p, SATA_R[0:3]n, SATA_R[0:3]p, SATA_DET#[0:3], SATA_PWREN#[0:3], LPC_CLK, LPC_AD[0:3], LPC_FRAME#, LPC_SERIRQ#, LPC_DRQ#.

- The CPU **SHALL NOT DRIVE** these signals until it determines that there is not a Bus Stacking Error.
- If the system detects a bus stacking error, it must remain in reset and not drive these signals.
- The CPU must tolerate PCI Express signal levels on these signals during reset.

The rules for all host CPUs are detailed below and affect the operation of pins 52, 54, and 105 on PCIe/104 Connector A.

Table 4-4 Host CPU Stacking Rules

Host	53 STK0/WAKE#	54 STK1/PEG_ENA#	105 STK2/SDVO_DAT
Type 1	During Reset: 0 = Bus Stacking Error 1 = Normal Operation	0 = Enable PCIe x16 1 = Enable GFX(optional)	0 = Enable PCIe x16 1 = Enable GFX(optional)
Type 2	0 = Normal Operation 1 = Normal Operation	0 = Bus Stacking Error 1 = Normal Operation	0 = Normal Operation 1 = Bus Stacking Error

Table 4-5 Required Host Connector A Pin Configuration

Host Type	53 STK0/WAKE#	54 STK1/PEG_ENA#	105 STK2/SDVO_DAT
Type 1	Input (100K Pull-up)	Input (100K Pull-up)	Input (100K Pull-down)
Type 2	Input (100K Pull-up)	Input (1K Pull-up):	Input (100K Pull-down):

- All pull-ups described above must be to 3.3V that is derived from the +5V_Always supply. If a board does not have the appropriate supply, a Thevenin equivalent resistor divider may be used. All pull-downs are to ground.

4.3. Peripheral Configuration Rules

The signals that need special consideration are: SATA_T[0:3]n, SATA_T[0:3]p, SATA_R[0:3]n, SATA_R[0:3]p, SATA_DET#[0:3], SATA_PWREN#[0:3], LPC_CLK, LPC_AD[0:3], LPC_FRAME#, LPC_SERIRQ#, LPC_DRQ#.

- Peripheral cards **MUST NOT DRIVE** these signals while PE_RST# is asserted.
- The peripheral cards must tolerate PCI Express signal levels on these signals during reset.

Rules guiding peripheral boards are listed in Table 4-6.

Table 4-6 Peripheral Stacking Rules

Bus	Peripheral Interface	53 - STK0/WAKE#	54 – STK1/PEG_ENA#	105 – STK2/SDVO_DAT
Type 1	PCIe x16 or x8	Hi-Z During Reset	Short to GND	Open
Type 1	Alternate Function	Open	Open	1K to 10K Pull-up
Type 2	SATA, USB 3.0, LPC	Short to GND	Open	Open
Universal	PCIe x4	Hi-Z During Reset	10K Pull-down	Open
Universal	PCIe x1 or USB 2.0	Hi-Z During Reset	Open	Open

- All pull-ups described above must be to 3.3V that is derived from the +5V_Always supply. If a board does not have the appropriate supply, a Thevenin equivalent resistor divider may be used.
- A peripheral device must be able to be stacked above or below the Host. Therefore, the peripheral must be capable of selecting the TX, RX, and clock lines from the top connector or the bottom connector.
- If any link(s) from a Link group (PCI Express x1, PCI Express x4, PCI Express x8, USB 2.0, USB 3.0, or SATA) is used on the module, the other links in that group must be shifted to the appropriate positions.
- Any unused signals must be passed between top and bottom using no more than two vias and as short of a trace as possible.

4.4. Stack Configuration Examples

Figure 4-1 illustrates a stack down configuration using PCI/104-Express and PCI-104 peripheral modules. In this configuration the Connector A, PCIe/104, could be either Type 1 or Type 2.

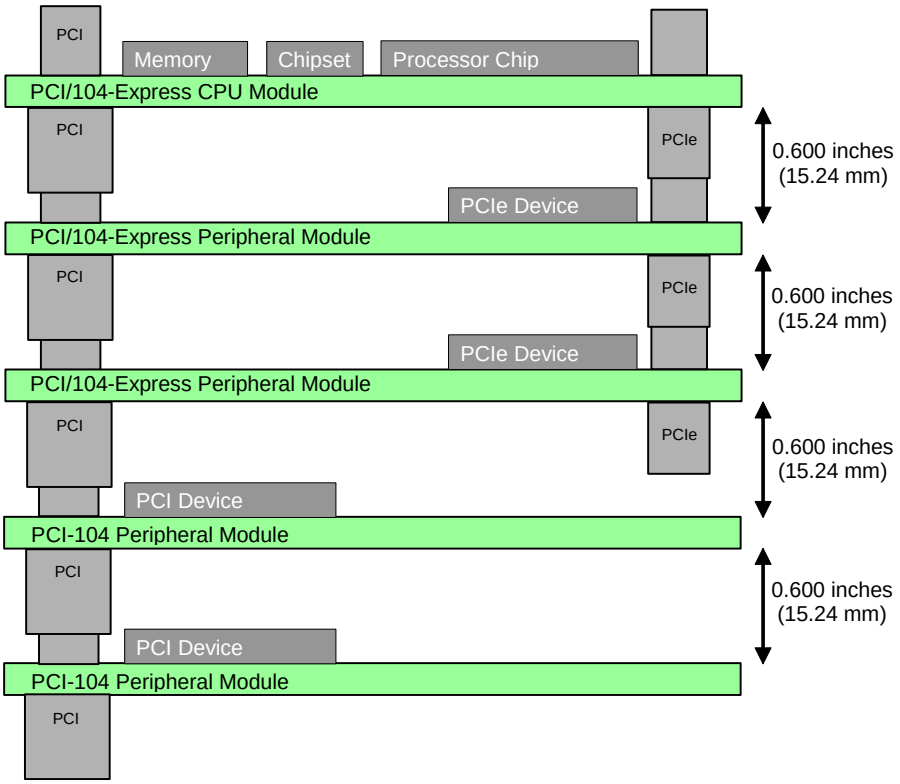


Figure 4-1: Type 1 or 2 Stack-DOWN Configuration Example

Figure 4-2 illustrates putting PCIe/104 and PCI/104-Express peripheral modules on an EPIC Host board. In this configuration Connector A, PCIe/104, could be either Type 1 or Type 2.

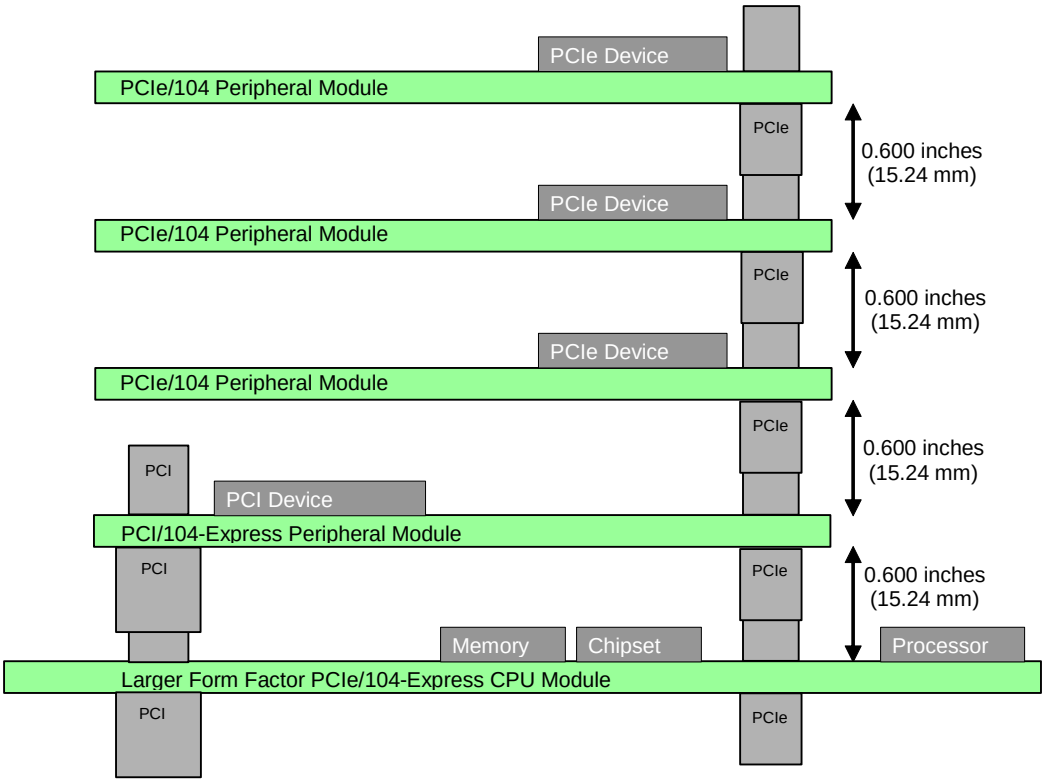


Figure 4-2: Type 1 or 2 Stack-UP Configuration Example with EPIC Host Baseboard

Figure 4-3 illustrates a stack with PCIe/104, PCI/104-Express and PCI-104 peripheral boards. In this configuration Connector A, PCIe/104, could be either Type 1 or Type 2.

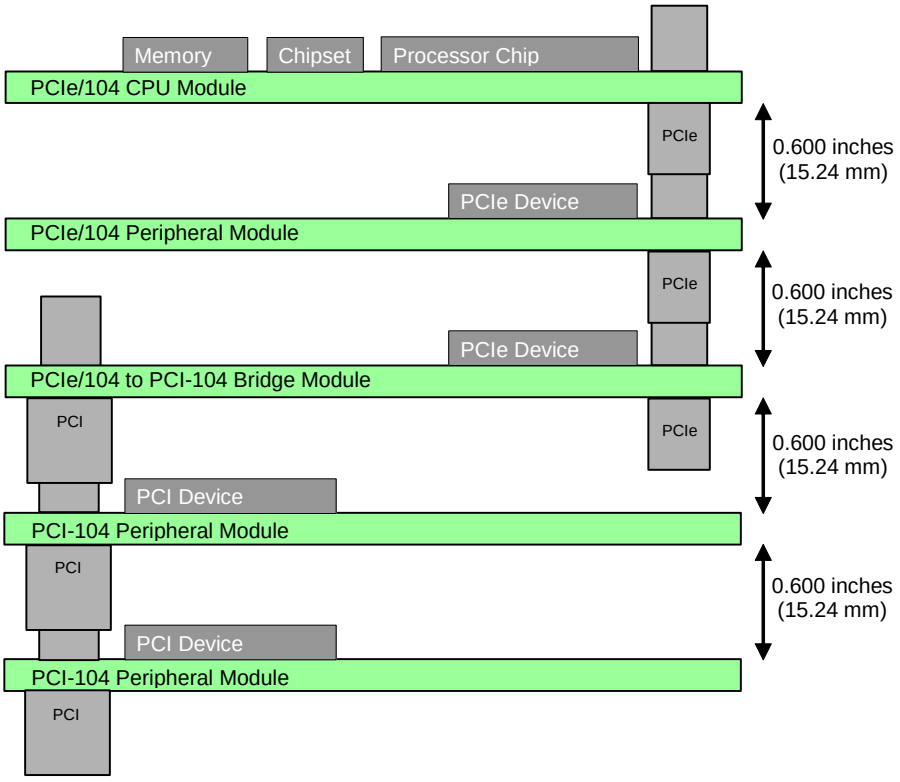


Figure 4-3 PCIe/104 with a PCI Express to PCI Bridge

Figure 4-4 illustrates a stack that has PCI/104-Express Host with the PCIe/104 bus connected top and bottom with PCIe/104, PC/104-*Plus*, and PCI-104 peripherals. In this configuration Connector A, PCIe/104, could be either Type 1 or Type 2. Because of the requirement that each type of bus must completely reside on one side of the Host in order to avoid bus splits and signal stubs, only PCI-104 and PCIe/104 modules can be used in this configuration. In this example all of the PCI-104 boards are on the bottom side of the Host and all of the PCIe/104 modules are on the top side of the Host. The reverse configuration is also valid.

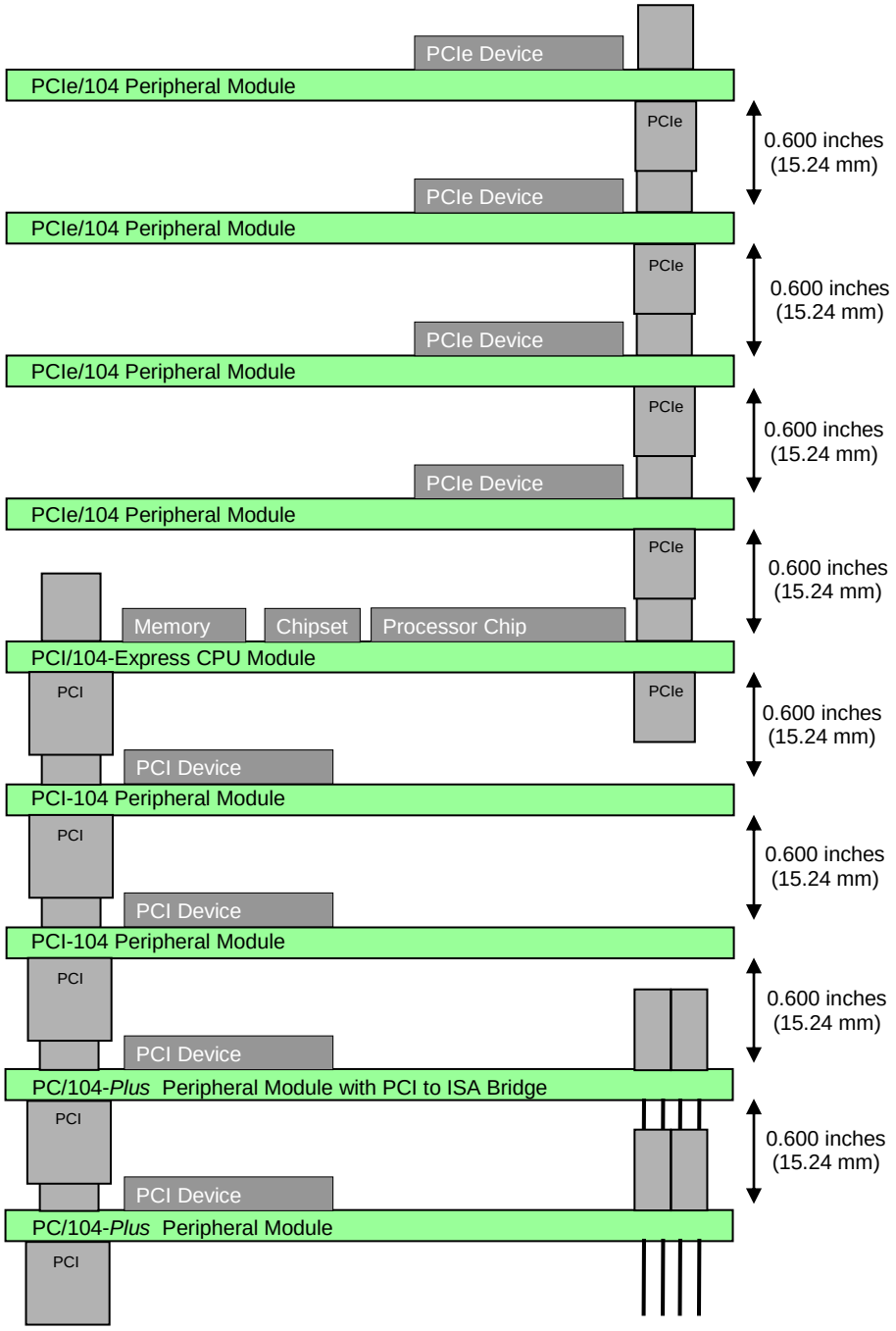


Figure 4-4: PCI/104-Express Combined Stack-UP and Stack-DOWN Configuration Example

Figure 4-5 illustrates a Host with a PCIe/104 Type 1 connector going down and a PCIe/104 Type 2 connector going up. The Host does not have the top and bottom busses connected. Type 1 and Universal Devices are stacked below the Host. Type 2 and Universal Devices are stacked above the Host.

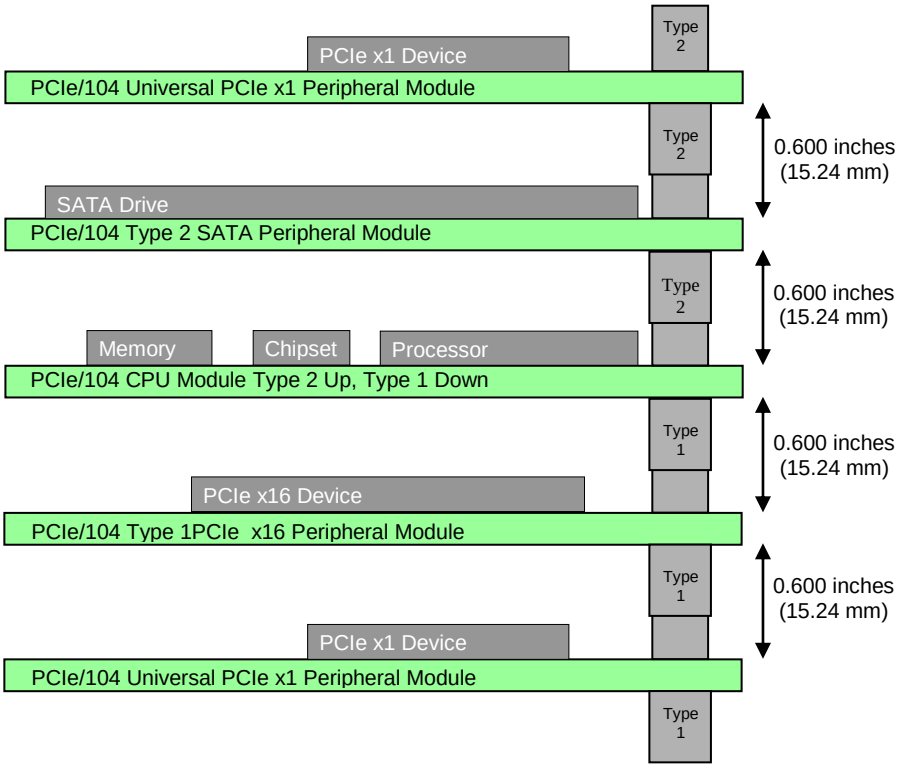


Figure 4-5: PCIe/104 Type 1 Stack-down and Type 2 Stack-up Configuration Example

Figure 4-6 illustrates a Host with a PCIe/104 Type 2 connector going down and a PCIe/104 Type 2 connector going up. The Host does not have the top and bottom busses connected so, as in this example, it can support up to 4 SATA Devices. In this example Type 2 and Universal Devices are stacked either above or below the Host or both at the same time.

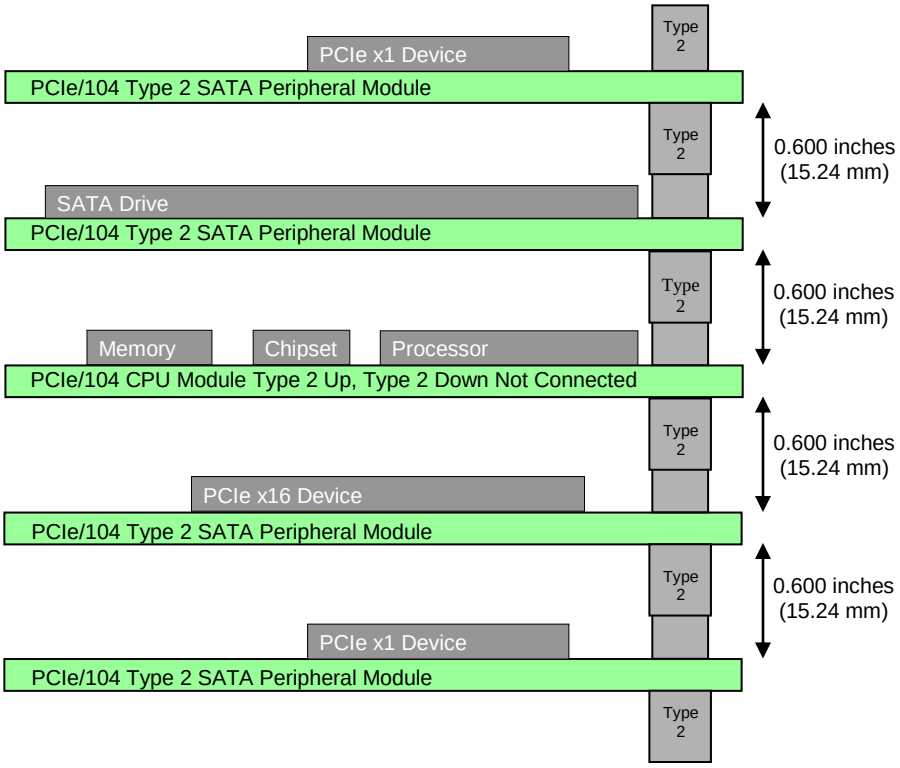


Figure 4-6: PCIe/104 Type 2 Stack-down, Type 2 Stack-up Busses Not Connected Configuration Example

5. ELECTRICAL SPECIFICATION

5.1. Power and Ground

5.1.1 Connector A, PCIe/104, Power Capabilities

The power rails on Connector A are +5V_SB, +3.3V, +5V, and +12V. The +5V and +12V are carried on central conductor planes which are dispersed among the three banks of Connector A. The +5V_SB is carried on individual pins. The current carrying capacities of the central panes and pins are shown in Table 5-1 below. Current values include a 20% industry standard de-rating factor at 85 °C. Note that at lower temperatures the current carrying capacities increase. There is a 2.9 to 1 ratio of current ground to current voltages which helps ensure good current paths.

Table 5-1 Connector A Power Delivery

Voltage	Minimum Voltage (V)	Maximum Voltage (V)	Number of Pins	Current per Pin (A)	Total Current (A)	Total Power (W)
+3.3V	3.00	3.60	2	1.8	3.6	11.9
+5V	4.75	5.25	2 planes	8.4	16.8	84.0
+12V	11.40	12.60	1 plane	8.4	8.4	100.8
+5V_SB	4.75	5.25	2	1.8	3.6	18.0
GND	n/a	n/a	46	1.8	82.8	n/a

Standby power is supplied for wake capabilities. Because of the limited amount of power available during standby, it is important for Device cards to be designed to minimize power consumption from the standby rail. Note that during full power operation, the voltage on the Standby rail may exceed the voltage on the +5V rail. Therefore, if powering devices from both the standby and the +5V rail, care must be taken not to exceed the current limits of the Standby rail during normal operation. The +12V rail is intended to provide additional power for high power devices

5.1.2 Connector B, PCI-104, Power Capabilities

Table 5-2 Connector B Power Delivery

Voltage	Minimum Voltage (V)	Maximum Voltage (V)	Number of Pins	Current per Pin (A)	Total Current (A)	Total Power (W)
+3.3V	3.00	3.60	10	1.0	10.0	33.0
+5V	4.75	5.25	8	1.0	8.0	40.0
+12V	11.4	12.6	1	1.0	1.0	12.0
-12V	-12.6	-11.4	1	1.0	1.0	12.0
GND	n/a	n/a	23	1.0	23.0	n/a

5.1.3 Total PCIe/104 Power Capabilities (Connector A Only)

Table 5-3 Connector A Power Delivery

Voltage	Minimum Voltage (V)	Maximum Voltage (V)	Total Current (A)	Total Power (W)
+3.3V	3.00	3.60	3.6	11.9
+5V	4.75	5.25	16.8	84.0
+12V	11.40	12.60	8.4	100.8
+5V_SB	4.75	5.25	3.6	18.0
GND	n/a	n/a	82.8	n/a

5.1.4 Total PCI/104-Express Power Capabilities (Connector A and B)

Table 5-4 Combined Connector A and B Power Delivery

Voltage	Minimum Voltage (V)	Maximum Voltage (V)	Total Current (A)	Total Power (W)
+3.3V	3.00	3.60	13.6	44.9
+5V	4.75	5.25	24.8	124.0
+12V	11.40	12.60	9.4	112.8
-12V	-12.6	-11.4	1.0	12.0
+5V_SB	4.75	5.25	3.6	18.0
GND	n/a	n/a	105.8	n/a

5.2. AC/DC Signal Specifications

5.2.1 Stackable PCI Express Expansion Bus

For full details on the electrical requirements for the PCI Express bus, reference the *PCI Express Base Specification* referenced in Section 1.9.7.

5.2.1.1 Power and Ground Pins

Power and ground planes are shared among all of the interfaces on Connector A. See Section 2 for more details.

5.2.2 Stackable PCI Expansion Bus

For full details on the electrical requirements for the stackable PCI bus, reference the PC/104-*Plus* or PCI-104 Specifications referenced in Section 1.9.7.

5.2.2.1 Power and Ground Pins

Power and ground planes are shared among all of the interfaces on Connector A. See Section 2 for more details.

5.2.3 System Management Bus (SMBus)

For full details on the electrical requirements for the SMBus, reference the *System Management Bus (SMBus) Specification* referenced in Section 1.9.7.

5.2.3.1 Power and Ground Pins

Power and ground planes are shared among all of the interfaces on Connector A. See Section 2 for more details.

6. MECHANICAL SPECIFICATIONS

6.1. Connector A

Samtec's QMS/QFS High Speed Interface series connectors were optimized for a 0.600" (15.24mm) stacking height and standoff tolerances. Additionally, an optional 22mm top connector was developed to allow additional height above the board. In both height options the bottom connector remains the same. An equivalent connector can be used.

6.1.1 Part Number

- Top Connector (Standard): ASP-129637-03 with 0.600 inch (15.24 mm) stack height
- Top Connector (Optional): ASP-142781-03 with 0.866 inch (22.00 mm) stack height
- Bottom Connector (Standard): ASP-129646-03 same for either stack height

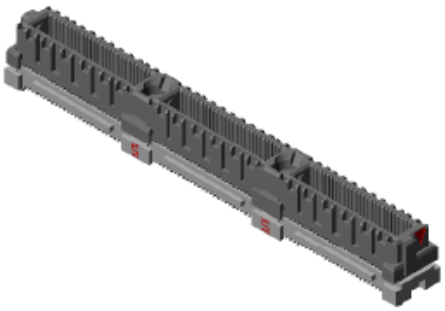


Figure 6-1 Standard Top Connector 0.600" (15.24mm) ASP-129637-03 or equivalent

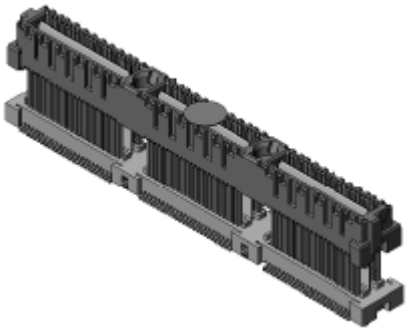


Figure 6-2 Optional Top Connector 0.866" (22.00mm) ASP-142781-03 or equivalent

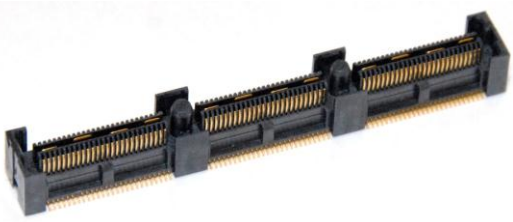
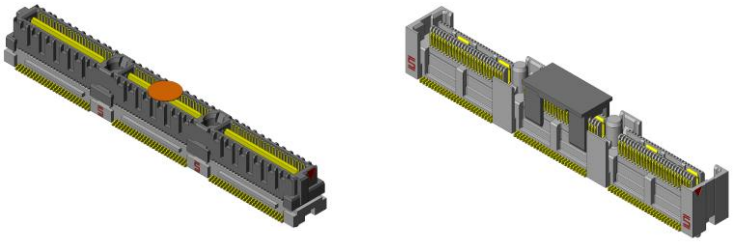


Figure 6-3: Bottom Connector ASP-129646-03 or equivalent



Top Connector **Bottom Connector**

Figure 6-4: Top Half and Bottom Half of Connector A Shown with Pick-and-Place Adapters

6.1.2 Connector A Specifications

MATERIALS

Housing:	Liquid Crystal Polymer
Terminal & Ground Plane Material:	Phosphor Bronze
Terminal Plating:	Au over 50μ" (1.27μm) Ni
Plane Plating:	Au over 50μ" (1.27μm) Ni
Terminal and Plane Tails:	Tin

CONTACT FINISH

Socket Interface:	30μ" Au
Terminal Interface:	30μ" Au
Underplate:	50μ" Ni

MECHANICAL PERFORMANCE

Insertion Force:	13.9 lbs initial & 16.8 lbs @ 100 cycles
Withdrawal Force:	9.8 lbs initial & 10.0 lbs @ 100 cycles
Normal Force @ nominal deflection:	69 grams

	Standard	Optional
Minimum stacking size:	14.8mm	21.56mm
Nominal stacking size:	15.24mm	22.00mm
Maximum stacking size:	15.50mm	22.26mm

Contact wipe (at nom. Height):	.044" [1.22mm]
Ground Plane wipe (at nom. Height):	.059" [1.50mm]
Durability:	50 cycles
Operating Temp:	-55 °C to 125 °C

ELECTRICAL PERFORMANCE

Positions	Three banks of 52 pins and 1 plane for 156 total pins and 3 planes
Contact Resistance (initial):	30 mOhms
Contact Resistance (@ 1,000 cycles):	50 mOhms
Contact Current Capacity:	1.8A at 85 °C and with 20% Industry Standard Derating Factor
Ground Plane Resistance:	0.5 mOhms
Ground Plane Current Capacity:	8.4A at 85 °C and with 20% Industry Standard Derating Factor
Dielectric Withstanding Voltage:	900 VAC
Working Voltage:	300 VAC
Insulation Resistance:	50,000 megaOhms

SOLDERABILITY

Maximum Processing Temperature:	230 °C for 60 seconds or 260 °C for 20 seconds

HIGH FREQUENCY PERFORMANCE

Differential Pair Impedance	100 Ohms nominal +/- 10%
Single-Ended Impedance	50 Ohms nominal +/- 10%
Differential Return Loss (SDD11):	-15dB @ 1.25 GHz; -8dB @ 5 GHz
Differential Insertion Loss (SDD21):	-1dB @ 1.25 GHz; -3dB @ 5 GHz
Differential Near End Crosstalk (SDD31):	-45dB @ 1.25 GHz; -35dB @ 5 GHz
Differential Far End Crosstalk (SDD41):	-45dB @ 1.25 GHz; -25 dB @ 5 GHz

6.1.3 Standard 0.600” (15.24mm) Top Connector A Mechanical Drawings

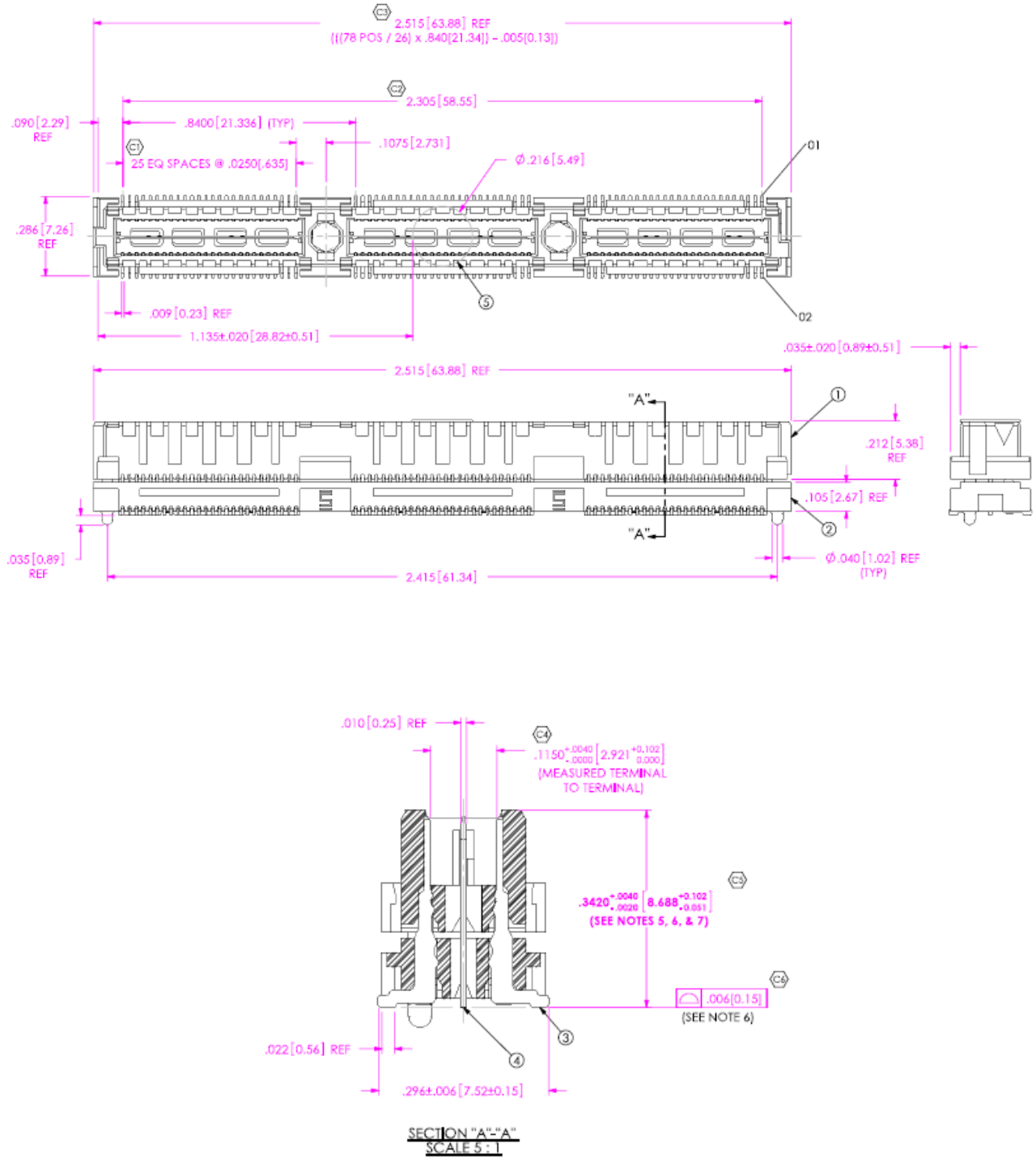


Figure 6-5: Standard 0.600” (15.24mm) Connector ASP-129637-03 or equivalent Mechanical Drawings

6.1.4 Optional 0.866” (22.00mm) Top Connector A Mechanical Drawings

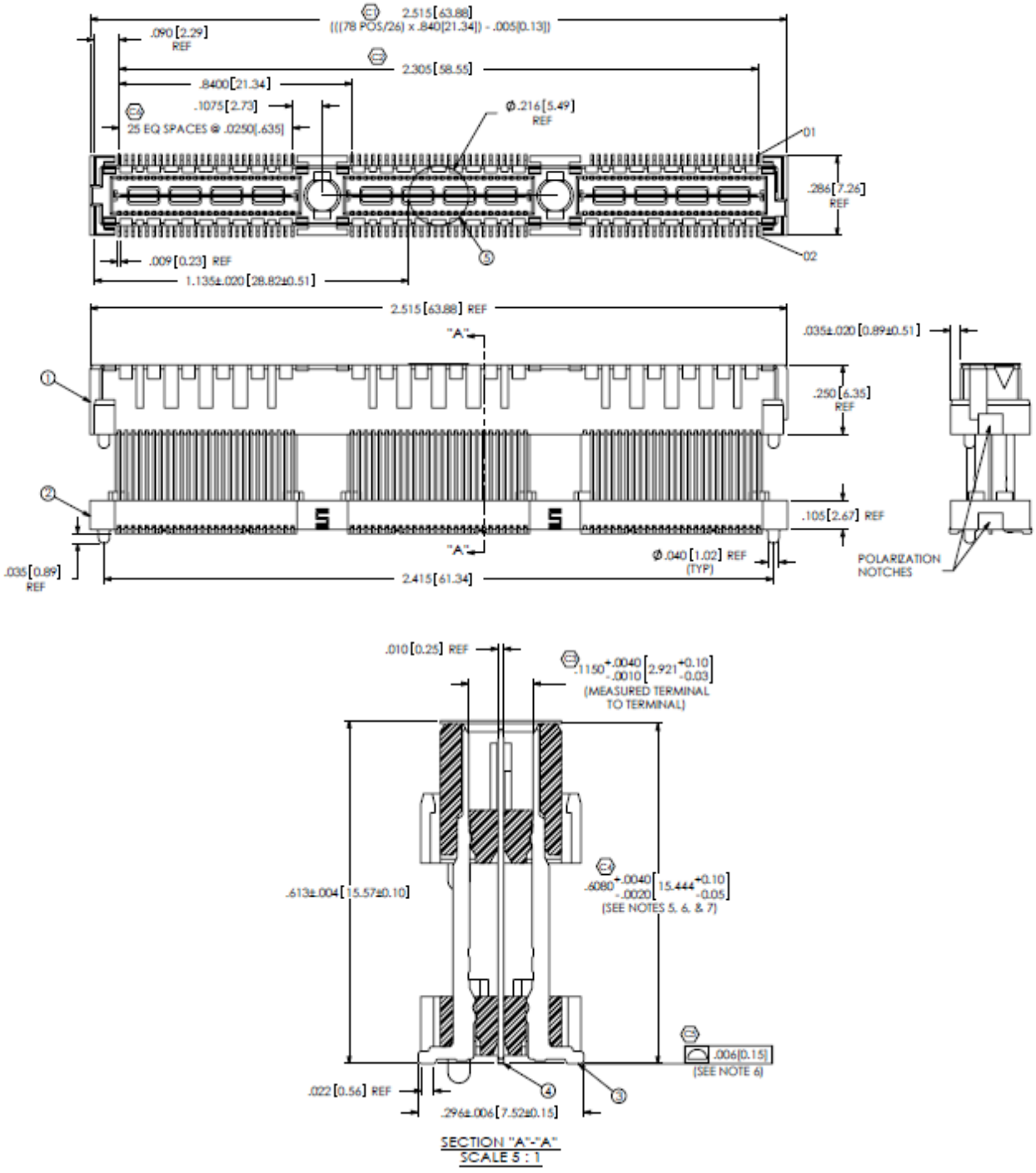


Figure 6-6 Optional 0.866” (22.00mm) Connector ASP-142781-03 or equivalent Mechanical Drawings

6.1.5 Standard ASP-129646-03 or equivalent (Bottom Connector) Mechanical Drawings

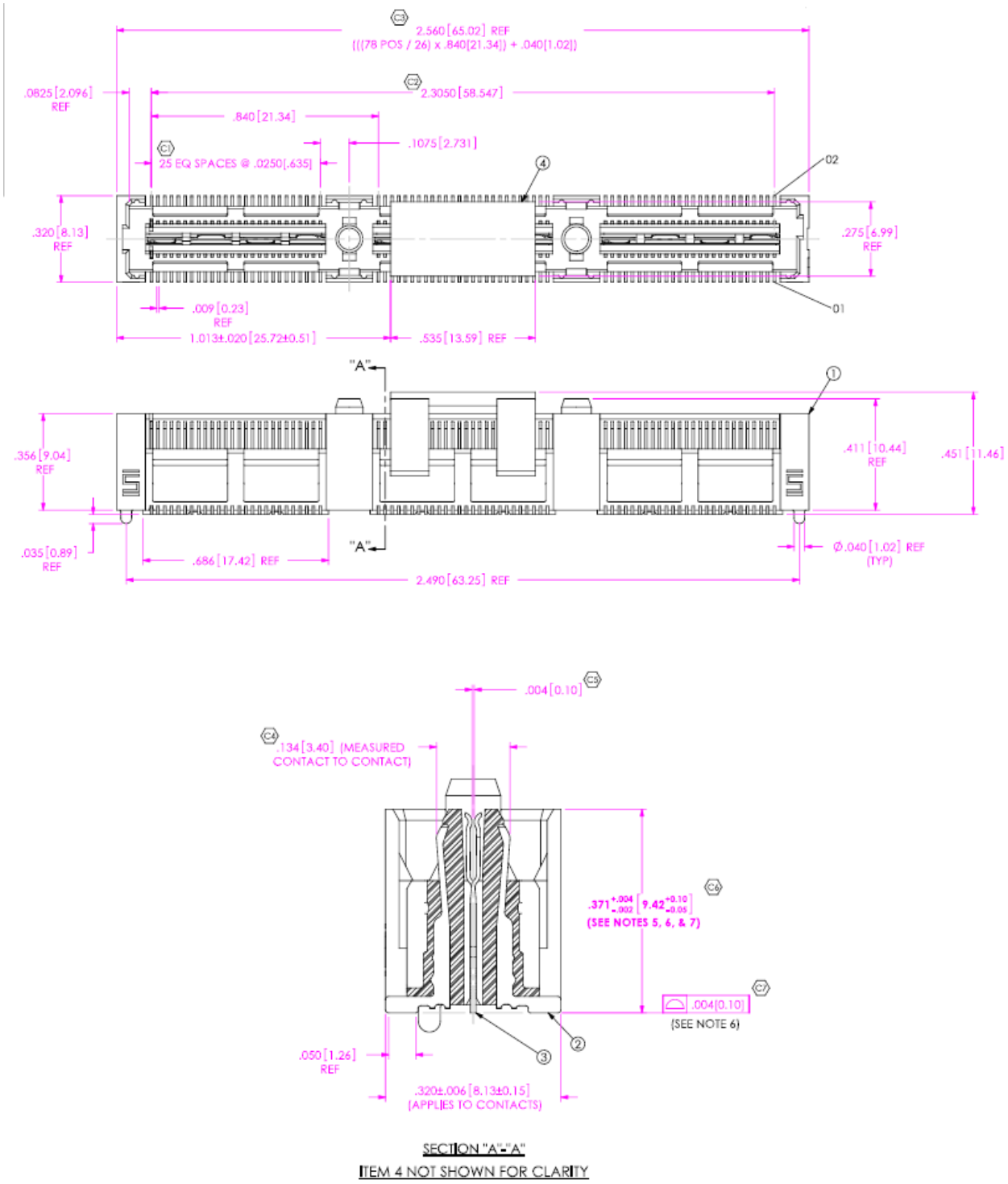


Figure 6-7: Standard ASP-129646-03 or equivalent Mechanical Drawings

6.2. Connector B

Connector B is the standard PCI bus that is used on PC/104-*Plus* and PCI-104 modules. See the PC/104-*Plus* or PCI-104 Specification for mechanical specification details of the connector.

6.3. Board Layout & Dimensions

6.3.1 PCIe/104 Layout & Dimensions

The outer mechanical dimensions for this module are identical to PCI/104-Express Specification with the exception of the removal of the PCI connector and some modifications to the I/O connector area.

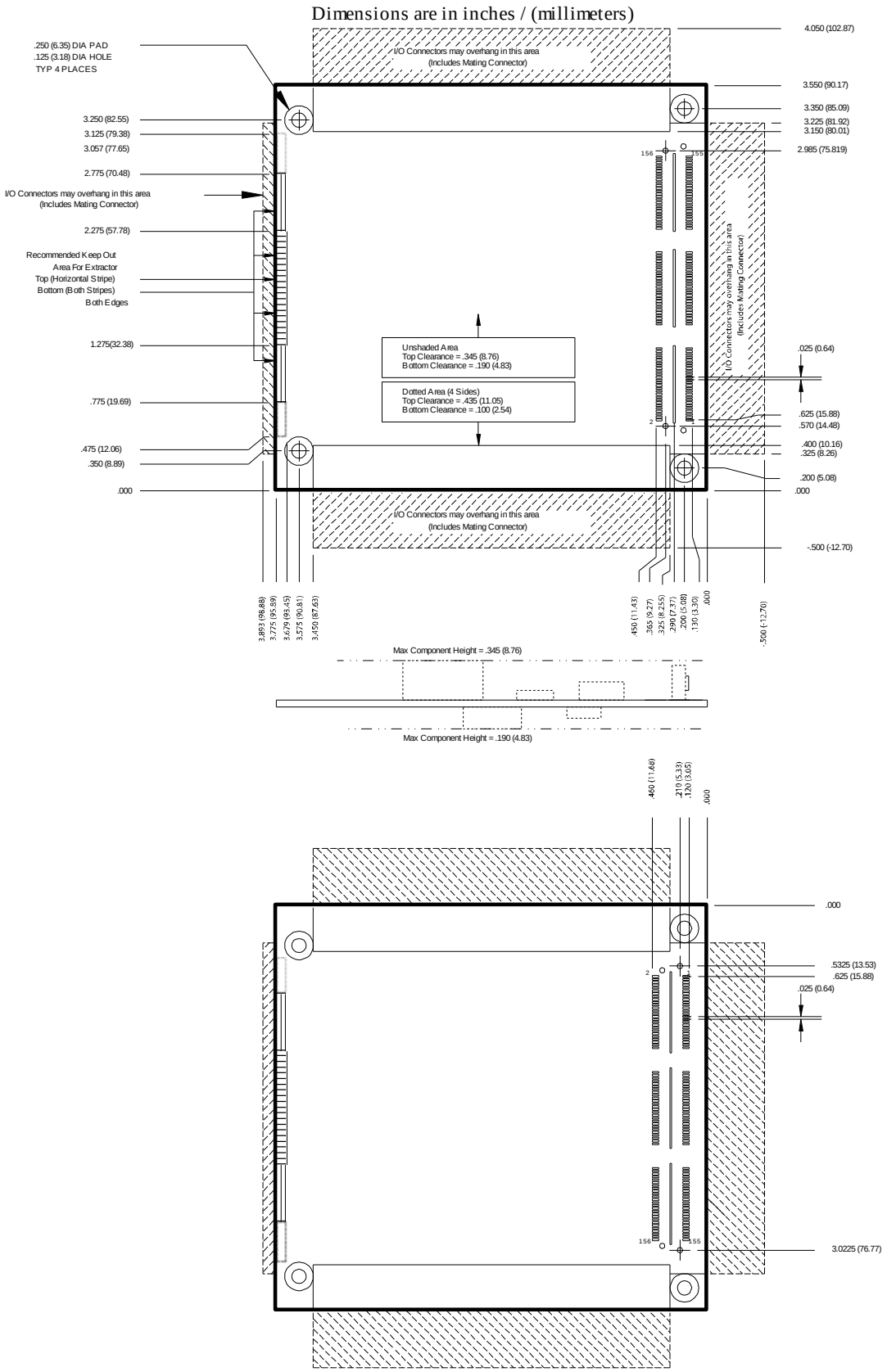


Figure 6-8 PCIe/104 Module Dimensions

6.3.2 PCI/104-Express Layout & Dimensions

The outer mechanical dimensions for this module are identical to PC/104-*Plus* Specification with the exception of the added connector (J3) and some modifications to the I/O connector area, and changes to the component height restrictions. The component height on the top has been reduced from 0.435" to 0.345" and the bottom has been increased from 0.100" to 0.190". Exceptions are the three regions on the sides of the module (indicated by the dotted region in Figure 6-9 which have a maximum height of 0.435" for the top and 0.100" for the bottom.

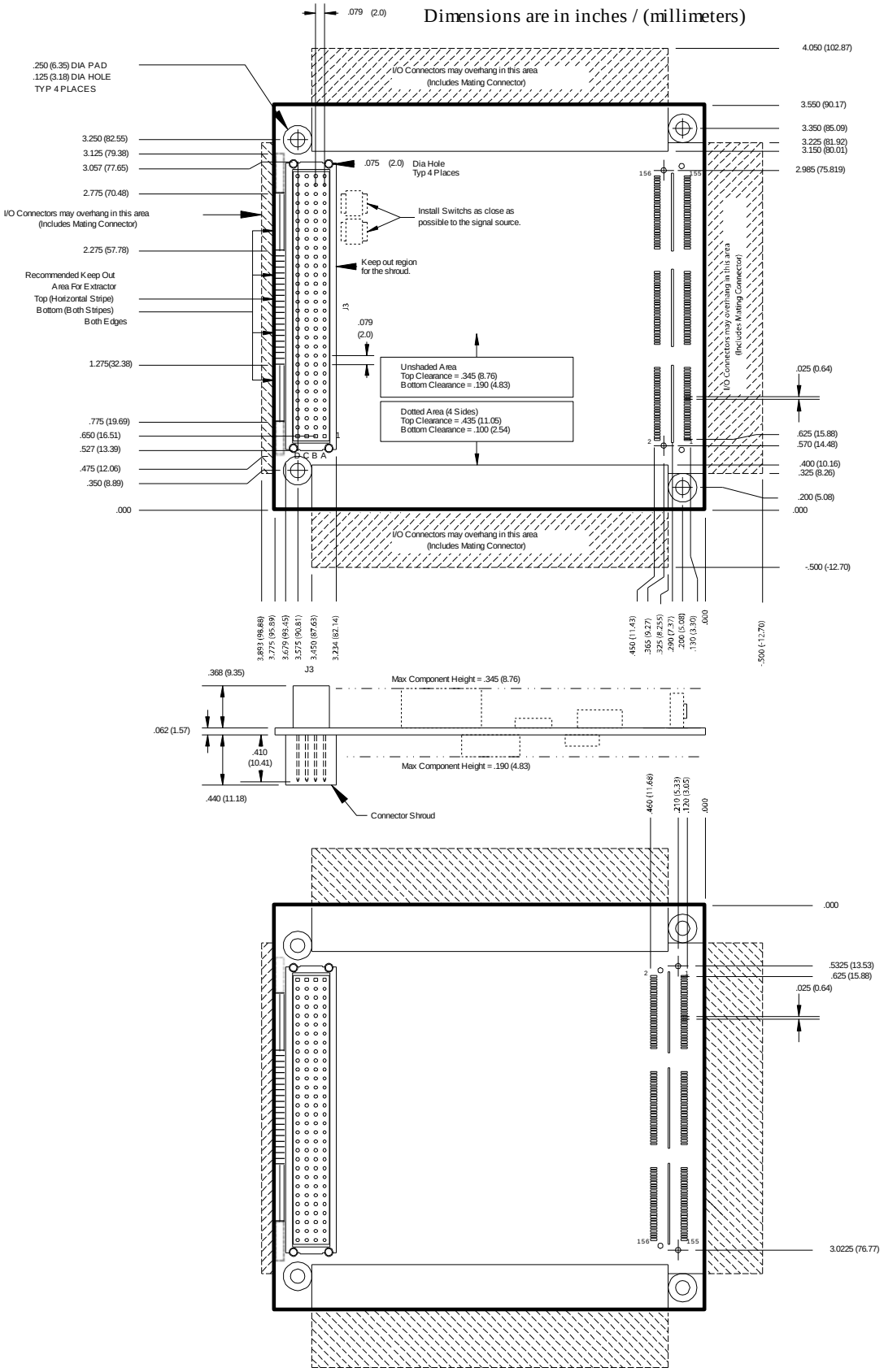


Figure 6-9 PCI/104-Express Module Dimensions

6.3.3 Connector A Placement Details

Since the QFS (ASP-129646-03) connector is larger than the QMS (ASP-129637-03), the QFS was used to determine the placement of both the QFS and the QMS. The maximum width of the QFS is determined by the recommend solder pad size and placement which is larger than the outer plastic dimensions of the QFS connector. The connector was lined up so that the base of the bottom solder pad lined up with the bottom of the AT ISA connector found on the PC/104 and PC/104-*Plus* form factors. This allows the retention of the traditional keep out region. With this placement the centerline of the connector (which placement should be based on) is located at 0.290 inches (7.37 mm) from the edge of the board.

The horizontal positioning of the QFS connector was calculated by positioning it in the center of the PCB and rounding off to a reasonable even multiple of 0.025 inches (0.635 mm) since this is the distance between two solder pads. The result was the first solder pad being located 0.625 inches (15.875 mm) from the left edge of the PCB as shown in Figure 6-10.

With the placement of the bottomside QFS connector, the QMS connector placement points are determined. The vertical placement point for the QMS is the same as that for the QFS which is 0.290 inches (7.37 mm) from the edge of the PCB to the center planes of the connector.

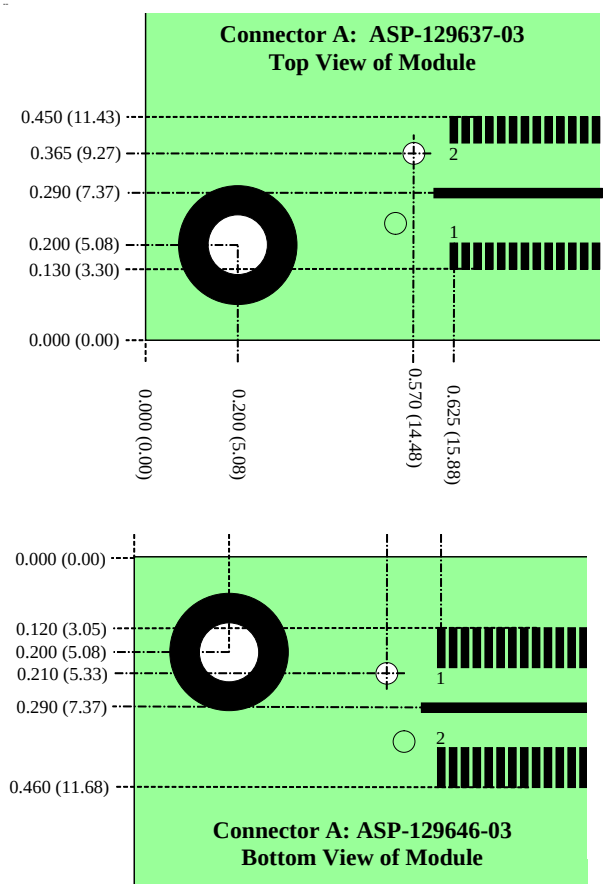


Figure 6-10: Top Side and Bottom Side Views of Connector Placements

Dimensions are in inches / [millimeters]

6.4. Standoff

Standoffs are used to ensure stacked boards retain their connectivity. The standoffs are preferably made from stainless-steel to provide for maximum strength and height tolerance. Pads must be provided for the standoffs, with the same plating as the pads for the PCI Express connectors.

All critical dimensions are listed. It is up to the user to define the thread type. The height of the standoff shall be 0.600 inches ±0.005 inches (15.24mm ±0.127mm).

Optionally, 22mm standoffs are to be used with the optional 22mm connector and they shall be 0.866 inches ±0.005 inches (22.00mm ±0.127mm) all other dimensions remain the same.

The width of the standoff must be able to fit on the Standoff pad called out on the Board Layout & Dimensions Section. The width of the threaded section must be able to fit into the standoff pad hole called out in the Board Layout & Dimensions Section.

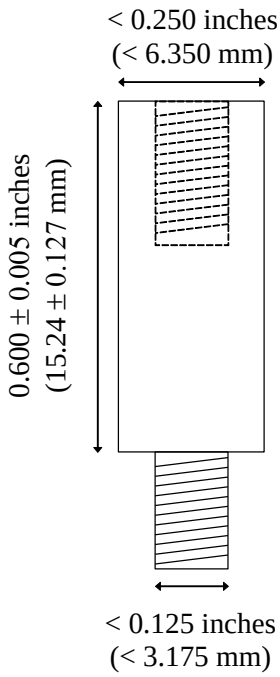


Figure 6-11: Standoff Mechanical Dimensions

APPENDIX A: PC/104 BRIDGE CARD

While advancing the PC/104 family of specifications, maintaining the stackable PCI bus was chosen over the stackable ISA bus for two reasons. First, many current and most future modern chipsets support both PCI and PCI Express. None support ISA. Second, backward compatibility to PC/104, PC/104-*Plus*, and PCI-104 is mechanically easier to achieve if the stackable PCI bus is retained over the stackable ISA bus.

To realize the stackable ISA bus, one merely needs to create a single board PCI-to-ISA bridge module using off-the-shelf PCI-to-ISA bridge chips or FPGA cores. This will get a basic ISA bus without DMA or IRQs. With the addition of three signals (SDMA_REQ, SDMA_GNT, and SIRQ) which are present on many chipsets and can be cabled to a bridge board, a full ISA bus can be realized for complete backward compatibility to all PC/104 specifications without any mechanical or electrical interference or deficiency issues.

And since the ISA bus is created using a PCI-to-ISA bridge chip, it is a natural electrical and mechanical extension to create the ISA bus off of the PCI expansion bus to support the number of ISA legacy cards already on the market. If the ISA bus was retained then creating a PCI bus off of the PCI Express bus would be easy electrically, but mechanically you have problems because the both the PCI expansion bus and the PCI Express expansion bus would reside in the same location. This would then require a two board solution to support the number of PC/104-*Plus* and PCI-104 cards already on the market.

A.1 Bridge Module Configurations

The PCI-to-ISA Bridge module has three possible configurations: Basic, Stack-UP only, and Stack-DOWN Only. Because of the heights of the Q2 (PCI/104-Express and PCIe/104) connectors and the ISA Bus (PC/104-*Plus*) connector and because they reside in the same general location, interference can occur if a PCI-to-ISA Bridge module is placed next to PCI/104-Express or PCIe/104 module.. In this case a Stack-UP Only or a Stack-DOWN Only version must be used. If there is a PCI-104 module between the PCI-to-ISA Bridge module and a PCI/104-Express or PCIe/104 module then a Basic configuration can be used.

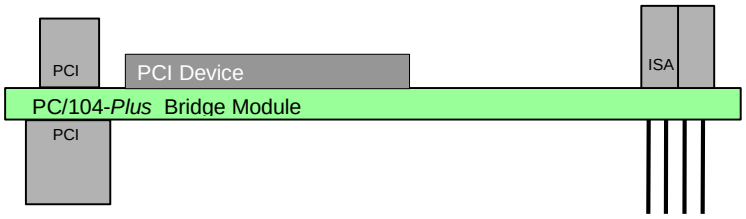


Figure 6-12: Basic Configuration of the PCI-to-ISA Bridge Module

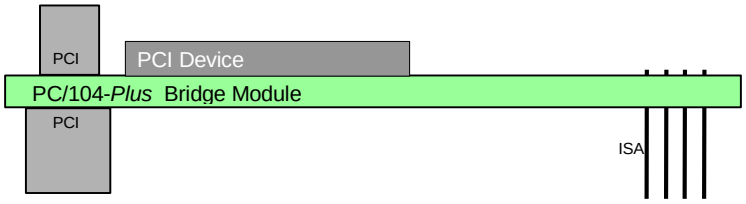


Figure 6-13: Stack-DOWN Configuration of the PCI-to-ISA Bridge Module

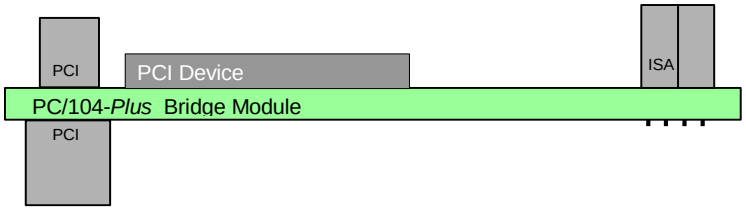


Figure 6-14: Stack-UP Configuration of the PCI-to-ISA Bridge Module

A.2 Stack Configuration Examples

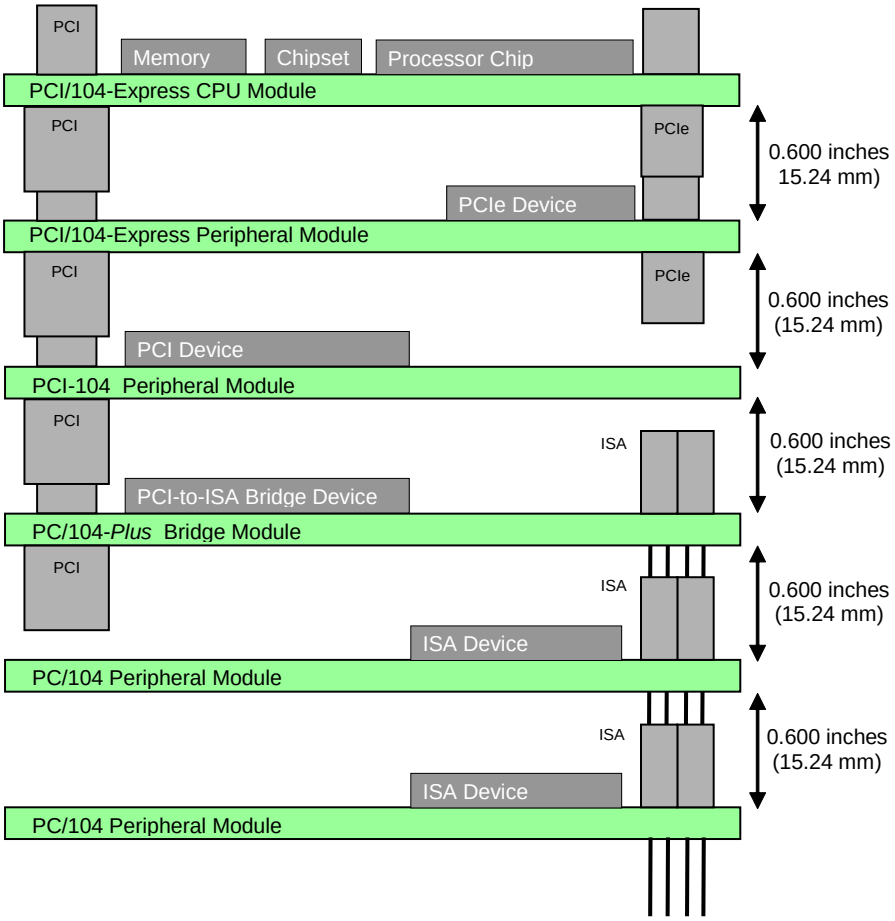


Figure 6-15: Stack-DOWN Configuration Example

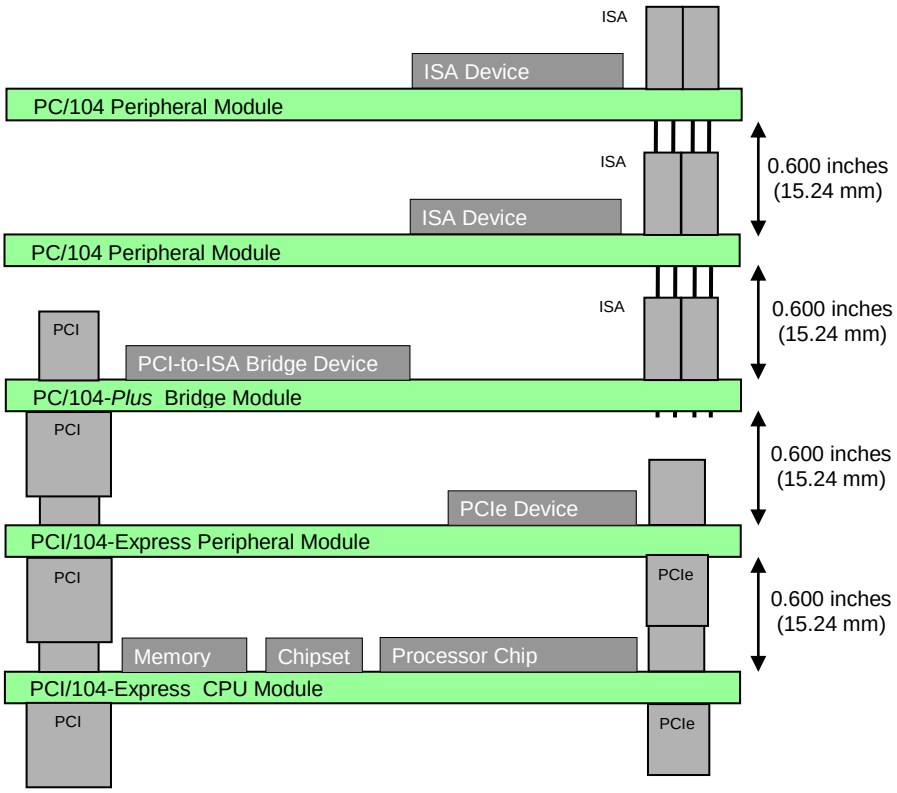


Figure 6-16: Combined Stack-UP Configuration Example

APPENDIX B: EPIC FORM FACTOR – PCI/104-Express Placement

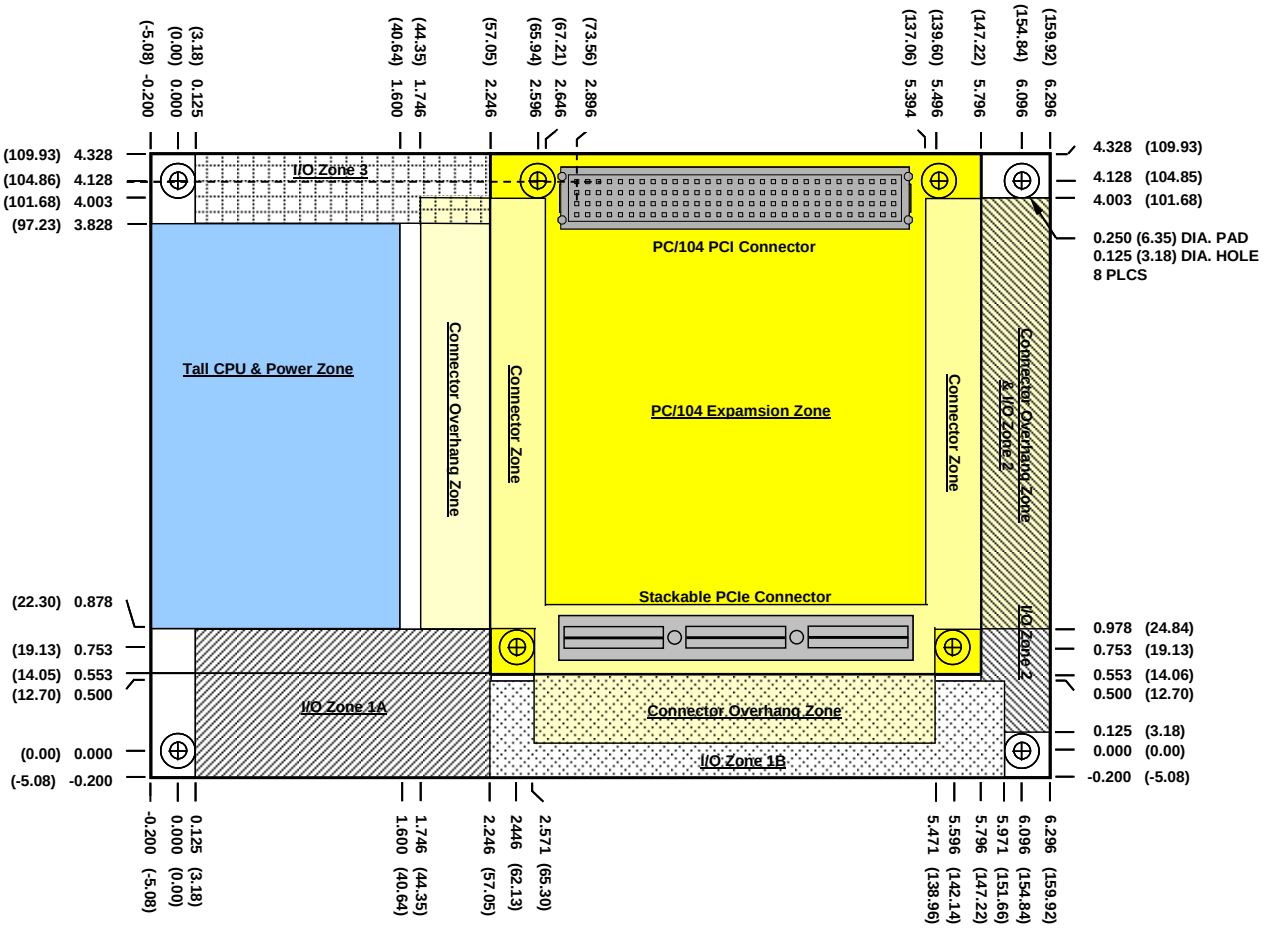


Figure 6-17: EPIC with PCI/104-Express

APPENDIX C: EBX FORM FACTOR – PCI/104-Express Placement

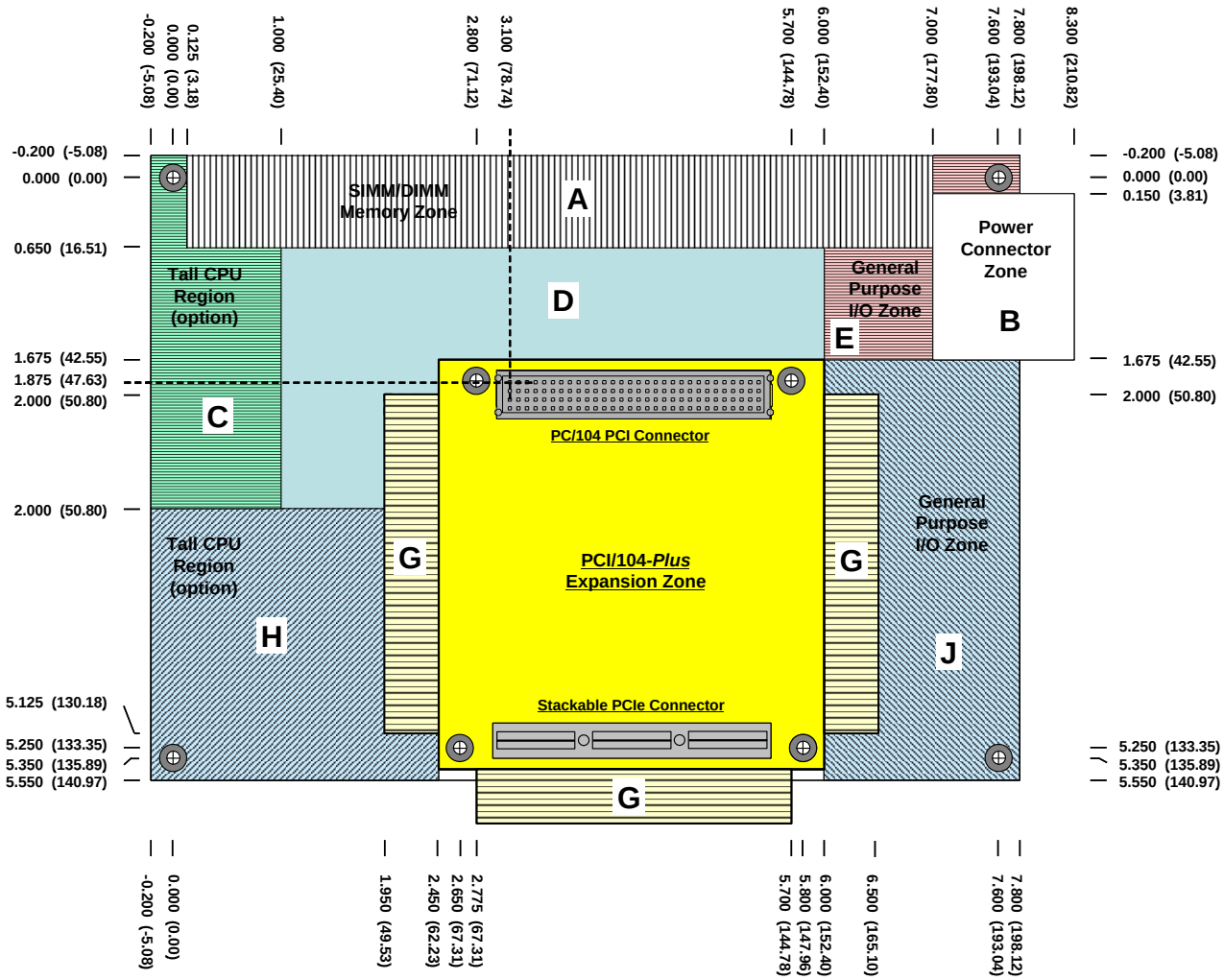


Figure 6-18: EBX with PCI/104-Express